ISSN 0970-3993

81
January
1990

Rs. 10.00

elektor INDIA
electronics

PROJECTS:

- 6502 TRACER
- LF/HF SIGNAL TRACER
- INTEGRATED-CIRCUIT TESTER
- LOUDSPEAKER PEAK INDICATOR

CUMULATIVE INDEX – 1989

SUPPLEMENT ON
ASIA'S BIGGEST FAIR
ELECRAMA-90

Volume – 8 Number – 1
January 1990

Publisher: C.R. Chandarana
Editor: Surendra Iyer
Circulation: **Advertising**: J. Dhas
Production: C.N. Mithagari

Address:
ELEKTOR ELECTRONICS PVT. LTD.
52, C Proctor Road, Bombay-400 007 INDIA
Telex: (011) 76661 ELEK IN

OVERSEAS EDITIONS

Elektor Electronics (Publishing)
Down House, Broomhill Road,
LONDON SW18 4JQ
Editor: Len Seymour

Elektor sarl
Route Nationale; Le Seau; B.P. 53
59270 Bailleul – France
Editors: D R S Meyer;
G C P Raedersdorf

Elektor Verlag GmbH
Süsterfeld-Straße 25
5100 Aachen – West Germany
Editor: E J A Krempelsauer

Elektor EPE
Karaiskaki 14
16673 Voula – Athens – Greece
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Elektuur B.V.
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Electronic Press AB
Box 5505
14105 Huddinge – Sweden
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Printed at : Trupti Offset Bombay - 400 013

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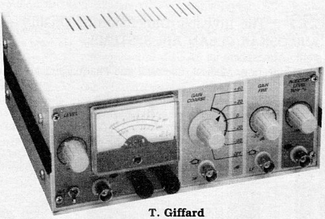
LF/HF SIGNAL TRACER



T. Giffard

Second in our series of budget test equipment, the signal tracer presented here is a versatile instrument that offers a signal generator, a tracing amplifier, a millivolt meter and an AF monitor amplifier with loudspeaker output in a single, compact enclosure. These functions make the instrument particularly suited to testing, servicing and aligning a wide range of electronic equipment.

One particularly useful feature of the present sinal tracer is that every one of its functions mentioned above is available separately. For instance, the preamplifier with accurately defined, selectable, gain may be used as a 'drop-in' amplifier which is often required for measurements at low signal levels. Similarly, the sine-wave oscillator, the millivolt meter and the monitor amplifier may be used on their own.

Input circuit

The signal tracer has two inputs — see the circuit diagram in Fig. 1. The LF (low frequency) input socket is connected direct to a high-impedance (1 MΩ) resistor lad-

LF/HF SIGNAL TRACER

Measurement ranges	
Alternating voltage:	−40 dB (10 mV) −20 dB (100 mV) 0 dB (1 V) +20 dB (10 V) +40 dB (100 V)
Bandwidth:	15 Hz to 350 kHz (−3 dB) 30 Hz to 200 kHz (−1 dB)
Input impedance:	>1 MΩ
Measurement amplifier	
Output impedance:	600 Ω
Bandwidth:	see 'Measurement ranges'
Amplification:	100 (40 dB) (10 mV range, attenuator at 0 dB)
Monitor amplifier	
Bandwidth:	35 Hz to 21 kHz (−3 dB)
Output voltage:	0 V to 6 V_{pp} (2.2 V_{rms})
Nominal load resistance:	8 Ω
Nominal output power:	560 mW
Sine-wave generator	
Frequency:	1 kHz
Output amplitude:	0 V to 4.25 V_{pp} (1.5 V_{rms})
Distortion:	less than 0.05% (2nd harmonic)
Output impedance:	max. 3 kΩ
Power supply	
Input voltage (mains powered):	min. 11 VDC
Stand-by current @ 11 V:	5 mA (S_1 off) 18 mA (S_1 on)
Stand-by current @ 9 V (battery powered):	<0.1 μA (S_1 off) approx. 13 mA (S_1 on)
Maximum current consumption at nominal AF output power:	125 mA @ 9 V (battery-powered) 125 mA @ 8 V (mains-powered)

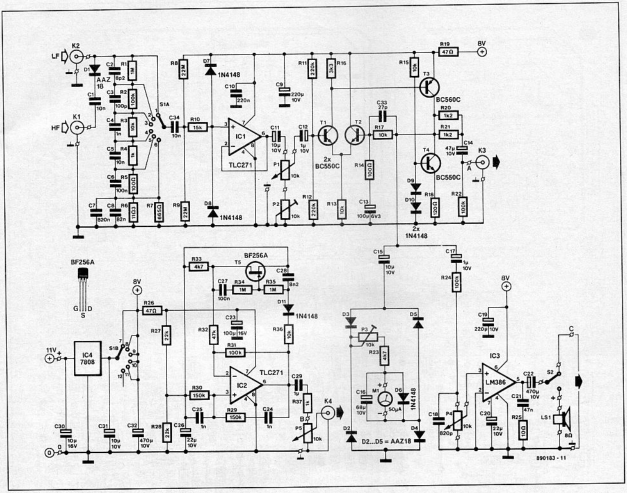


Fig. 1. Circuit diagram of the versatile signal tracer.

der network. The HF input also feeds this network via a germanium diode, D_1, and a coupling capacitor, C_1. The LF input socket is used for all alternating-voltage measurements. The HF input is intended for tracing amplitude-modulated (AM) high-frequency signals in receiver circuits. The diode and the coupling capacitor form an AM demodulator whose output signal is fed to the resistor ladder network. Next, level selection switch S_1 passes the signal to the input of IC_1. The AM demodulator is particularly suited to repair work on receivers and communications equipment, and enables amplitude-modulated audio and video signals at intermediate frequencies to be traced.

Double-pole rotary switch S_1 functions as a range selector (S_{1a}) and an on/off switch (S_{1b}).

The voltage range of both inputs is 0 V to 100 V, as determined by the relevant rating of the input capacitor. In theory, the lowest setting of the range switch (contact 6 of S_{1a}) creates a 1,000 V range. Apart from being far outside the voltage rating of the input capacitor, such a range has no practical use in combination with a millivolt meter having a dB (decibel) read-out. Switch positions 1 (10 mV) through 5 (100 V) form the normal ranges, divided into decades. The instrument is turned off by selecting position 6.

The 100 V range should be ample for most applications: after all, a peak voltage 100 V, supplied by an AF amplifier with 4 Ω output impedance, corresponds to a power output of no less than 1,250 W.

Diodes D_7 and D_8 protect the high-impedance input amplifier, IC_1, against voltage peaks greater than about 100 V. Resistor R_{10} and the two diodes can not, however, afford protection against continuous overvoltage. The input may be given a higher maximum input voltage by increasing R_{10}, but only at the cost of a significant bandwidth reduction.

The high input impedance (1 MΩ) of the signal tracer is inevitably coupled to a relatively large, negative, effect of stray capacitance associated with the resistors and the rotary switch. Capacitors C_2 through C_8 are provided to compensate this capacitance, and result in a 3 dB bandwidth of about 350 kHz.

A low-power CMOS opamp Type TLC271 is used as the input amplifier because it offers high input impedance and bandwidth when powered from a single supply rail. The required drive margin is ensured with potential divider R_8-R_9, which holds the + input of the opamp at about half the supply voltage. The high value of these resistors, 22 MΩ, ensures that the resistor ladder network is only lightly loaded.

Tracing amplifier

The output signal of the input amplifier, IC_1, is applied to a linear potentiometer, P_1, before it arrives at the input of the measurement amplifier, a discrete circuit around T_1 and T_2. Preset P_2 allows the range of P_1 to be set to about 20 dB, corresponding to the ranges of S_1. The potentiometer serves as a variable attenuator that enables a particular reference level to be set on the moving-coil meter. If, for instance, the reference level is set to 0 dB, the −3 dB and −6 dB levels are easily read from the meter scale.

The measurement amplifier has a bandwidth of about 800 kHz. The lower cut-off frequency is set to 16 Hz by C_{13}, the decoupling capacitor with feedback resistor R_{14}. A lower cut-off frequency would be achievable by a increasing C_{13}. This is not recommended, however, since it lengthens the stabilization period of the in-

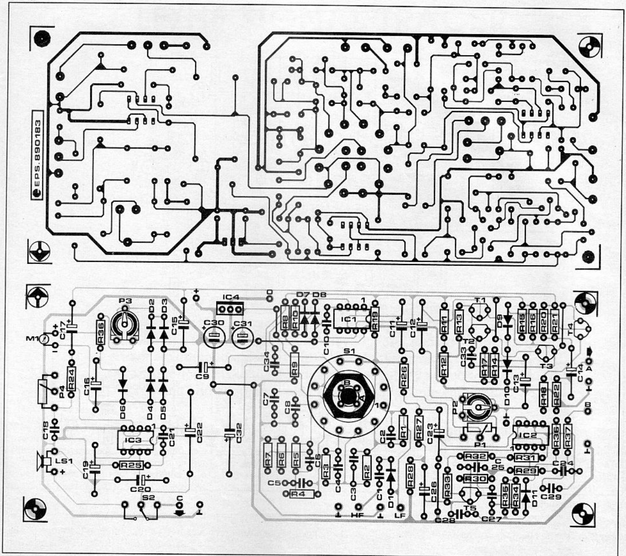


Fig. 2. The printed-circuit board is geared to the front-panel foil to give a compact and simple-to-build test instrument.

strument at power-on. With C_{13} at the given value, this stabilization period takes about 1 s. Feedback network R_{14}-R_{17} is dimensioned for a voltage amplification of 100 (40 dB).

The power stage of the measurement amplifier has an output impedance of about 600 Ω, as determined by R_{20}-R_{21}. The output signal is fed to socket K_3 via C_{14}, to the moving-coil meter circuit via C_{15}, and to a small monitor amplifier via C_{17}.

Summarizing the above, the circuit between the LF input socket and the 600 Ω output is a calibrated amplifier with high bandwidth, having a gain range of −40 dB to +40 dB in 20 dB steps, and an additional, continuously variable, 20 dB attenuator.

The meter circuit

The passive rectifier with germanium diodes D_2 – D_5 and moving-coil meter M_1 offers a relatively high bandwidth and a slightly logarithmic behaviour in the lower part of the meter range, which allows a dB scale to be made that is easily read (see the scale design in Fig. 3).

The Type AAZ18 diodes drop only 0.15 V at a forward current of 50 µA, and hardly affect the linearity in the lower part of the meter scale. Although other, similar, germanium diodes may be used, it should be noted that these may have slightly different characteristics, requiring the given meter scale to be modified.

The value of electrolytic capacitor C_{16} connected across the meter terminals has been chosen to stabilize the indication at relatively low frequencies without slowing down the average value conversion. Silicon diode D_6 protects the meter coil against voltages greater than about 0.6 V.

The meter circuit is simple to align: controls P_1 and S_1 are set to 0 dB, and preset P_3 is adjusted for full-scale deflection (f.s.d.) when an alternating voltage of 1 V_{rms} is applied to the LF input. The f.s.d. values in the other decade ranges of S_1 are 10 mV (−40 dB), 100 mV (−20 dB), 10 V (+20 dB) and 100 V (+40 dB). The meter may, of course, be provided with a voltage scale, provided this is corrected as required by the non-linear indication at small deflections.

The meter used for the prototype has a double scale, which was found particularly useful for AF measurements. The upper scale indicates dBs relative to 1 mW into 600 Ω, and has a 0 dB indication corresponding to 0.775 V. The f.s.d. value of 1 V is reached at an AF signal level slightly higher than +2 dB. On the lower dB scale, the 0 dB indication at f.s.d. is defined at a voltage level of 1 V.

Monitor amplifier

The monitor amplifier, IC_3, receives the output signal of the measurement amplifier via coupling capacitor C_{17}. The famil-

Parts list

Resistors:
R_{1} = 1M0; 1%
R_{2} = 100k; 1%
R_{3} = 10k; 1%
R_{4} = 1k0; 1%
R_{5} = 100Ω; 1%
R_{6} = 11Ω3; 1% (E96)
R_{7} = 665Ω; 1% (E96)
R_{8};R_{9} = 22M
R_{10} = 15k
R_{11};R_{12} = 220k
R_{13};R_{15};R_{17};R_{36} = 10k
R_{14} = 100Ω
R_{16} = 3k3
R_{18} = 120Ω
R_{19};R_{26} = 47Ω
R_{20};R_{21} = 1k2
R_{22};R_{24};R_{31} = 100k
R_{23};R_{33} = 4k7
R_{25} = 10Ω
R_{27};R_{28} = 22k
R_{29};R_{30} = 150k
R_{32} = 47k
R_{34};R_{35} = 1M0
R_{37} = 1k0

P_{1} = 10k linear potentiometer.
P_{2};P_{3} = 10k preset H
P_{4};P_{5} = 10k logarithmic potentiometer.

Capacitors:
C_{1} = 10n ceramic
C_{2} = 8p2
C_{3} = 100p
C_{4};C_{24};C_{25} = 1n0
C_{5};C_{34} = 10n
C_{6};C_{27} = 100n
C_{7} = 820n
C_{8} = 82n
C_{29} = 1µ0; MKT
C_{9};C_{19} = 220µ; 10 V
C_{10} = 220n
C_{11};C_{15} = 10µ; 10 V
C_{12};C_{17} = 1µ0; 10 V
C_{13} = 100µ; 6V3
C_{14} = 47µ; 10 V
C_{16} = 68µ; 10 V
C_{18} = 820p
C_{20};C_{26} = 22µ; 10 V
C_{21} = 47n
C_{22};C_{32} = 470µ; 10 V
C_{23} = 100µ; 16 V
C_{28} = 8n2
C_{30} = 10µ; 16 V; radial
C_{31} = 10µ; 10 V; radial
C_{33} = 27p

Semiconductors:
D_{1} – D_{5} = AAZ18
D_{6} – D_{11} = 1N4148
T_{1};T_{2};T_{4} = BC550C
T_{3} = BC560C
T_{5} = BF256A
IC_{1};IC_{2} = TLC271
IC_{3} = LM386
IC_{4} = 7808 or 7809

Miscellaneous:
S_{1} = PCB-mount dual-pole 6-way rotary switch.
S_{2} = miniature SPDT switch.
M_{1} = 50 µA moving-coil meter, e.g., Monacor Type PM-2, order code 29.0660.
LS_{1} = 8 Ω; 0.5 W loudspeaker.
K_{1};K_{2};K3;K_{4} = insulated BNC-sockets, e.g., Monacor order code 34.1880
Enclosure: e.g., Telet LC-850 (C-I Electronics).
PCB Type 890183

Front-panel foil Type 890183-F

iar Type LM386 AF amplifier chip is used in a standard application circuit with a Boucherot network, C_{21}-R_{25}, at its output. The input signal for the amplifier is reduced by R_{24} to a level where full drive coincides with f.s.d. on the meter. This level results in an output voltage of about 6 V_{pp} (2.2 V_{rms}), or 0.56 W into a load resistance of 8 Ω. The output signal is made available on the front panel of the instrument to enable an external loudspeaker or a pair of headphones to be connected.

Sine-wave oscillator

A high-quality sine-wave oscillator is provided to locate faulty AF circuits by means of the audible distortion they introduce. The oscillator consists of a Type TLC271 opamp with a Wien-bridge feedback circuit, C_{24}-R_{29} and C_{25}-R_{30}, to achieve amplitude stabilization. Feedback circuit R_{31}-R_{32}-T_{5} determines the closed-loop amplification of the oscillator. The drain-source junction of the FET forms a resistor whose value is a function of the output voltage rectified by D_{11} and fed back to the gate. Resistor R_{33} determines the minimum amplification when the FET is turned off completely, and at the same time linearizes the control characteristic.

The test oscillator has a distortion lower than 0.05% at a second harmonic level of −75 dB. The output frequency is about 1 kHz, and the output signal level is adjustable between 0 V and 1.5 V_{rms}.

Power supply

The on-board 8 V regulator allows an inexpensive mains adapter to be used with an output voltage of about 12 V. The 8 V regulator, IC_{4}, may be replaced by a 9 V Type 7809. It is also possible to power the instrument from a single 9 V battery, or a battery pack consisting of six 1.5 V monocells. When a battery is used, IC_{4} is omitted, and a wire is fitted to connect the holes provided for its input and output terminals.

Current consumption of the signal tracer depends mainly on the drive applied to the monitor amplifier. At relatively low volumes, the instrument draws 15 mA to 18 mA from a 9 V battery.

Construction

The printed-circuit board (Fig. 2) and the front-panel foil (Fig. 3) are both available ready-made, and make the signal tracer a simple-to-build project by reducing the wiring to a minimum. All sockets and controls are mounted direct on to the printed-circuit board, which is fitted vertically behind the front panel. The distance between the front panel and the printed-circuit board is determined by the length of the spindle of the rotary switch.

The rear panel of the enclosure holds the supply socket, the loudspeaker and the battery holder, if used.

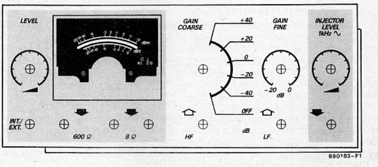


Fig. 3. Lay-out of the front-panel foil, which is available ready-made (shown at 60%).

THE DIGITAL MODEL TRAIN

PART 9: KEYBOARDS

by T. Wigmore

The keyboards used in the Elektor Electronics Digital Train System can each control eight turnouts (points) or signals or a mixture of these. They also enable other switching functions to be carried out (there are 16 impulse contacts or eight make/break contacts, depending on the decoder). In principle, any number of keyboards may be connected to the main board.

In essence, the system allows signals to be controlled in two different ways, in addition to the traditional one of using discrete switches. The most obvious one is with the aid of keyboards. Each of the turnouts (points) and signals then has its own switch that may be incorporated in a switchboard whose layout resembles that of the track.

Each keyboard (which can not be used with the Märklin system) contains 16 switches that enable eight turnouts or signals (each with two solenoids) or 16 sidings or loops (or seven turnouts and two sidings or loops, and so on) to be controlled. This is, of course , true only if the associated turnout and signal decoders or universal switching decoders are provided on the track. Any number of keyboards may simply be interconnected.

The RS232 interface (which will be the subject of next month's article) is the other way of controlling signals and turnouts, particularly when the track is an extensive one. It can, of course, only be used in conjunction with a computer.

The LEDs on the keyboards indicate the actual position of the signals and turnouts, irrespective of whether these are switched via the keyboard or via the RS232 interface. The keyboards may be deactuated by a suitable program via the interface to enable fully automatic operation.

Circuit description

It will be seen that the circuit diagram in Fig. 57 consists of two identical parts above and below connectors K_1 and K_2: in fact, it shows the circuit for two keyboards. This is also the case with the printed-circuit board: Fig. 59 thus holds two keyboard circuits. Operation will be described on the basis of the top half of Fig. 57.

Connectors K_1 and K_2 form the parallel keyboard bus; all their terminals bar one are interconnected. The exception is pin 10, which is the line that indicates whether a key is depressed.

Circuit IC_1 is a digital multiplexer. The eight switches on all connected keyboards are scanned simultaneously via lines A, B,C and E(nable) from the mother board (see Fig. 50 – Part 8). When a key is depressed, the associated input of IC_1 is logic high. When that input is selected, the $\overline{Y}$ output (pin 6) will go low, which is passed on to the mother board via gates N_2 and N_3. The yellow LED on that board then lights. All other keys are deactuated at that instant, because the associated switching instruction is be processed first.

When the Y output (pin 5) becomes active, the keyboard address buffer, IC_2, is enabled. The keyboard address (81 possible combinations, set with the aid of jumpers) is then placed on to the keyboard address bus. This address enables the system to deduce to which corresponding decoder the switching instruction must be sent.

The associated turnout sub-address that determines which of the eight decoder outputs has to become active is derived from the combined signals A, B and C with which the relevant depressed key was found. When a key is pressed, a switching instruction is placed on to the rails four times; when it is released, a reset instruction is sent four times to the same decoder address.

Circuits IC_3 (addressable bistables) and IC_4 (address comparator) provide a visual indication of the actual position of the signal or turnout.

When the system carries out a switching instruction (at most a few milliseconds after the key has been pressed), the switches are temporarily disabled and the microprocessor places the address just read on to the keyboard address bus. At the same time, an enable signal is given to the address comparator.

Only that keyboard of which a key was depressed will recognize its own address on the keyboard address bus via the Q-inputs of IC_4 . The address is present also at the P-inputs of IC_4. Output $\overline{P = Q}$ of IC_4 will go low and set or reset one of the four used bistables in IC_3, which causes the relevant LED connected at the output to just light or to just go out.

The address comparator, IC_4, is necessary to enable the LEDs to be driven when no key is pressed. This makes it possible for the new position of the turnout to be shown on the keyboard when the switching instruction for that turnout is given via the RS232 interface.

Each LED is associated with two switches and indicates the (normally bistable) position of the turnout.

The LEDs are energized via D_5 by the rectified but unregulated voltage to prevent an overload of the power rail for the logic circuits, which can occur when a large number of keyboards is used.

Gates N_1 and N_2 serve as priority selectors. Normally, both Do (data out – pin 10 of K_1) and Di (data in – pin 10 of K_2) are high. When a key is pressed, Do at the relevant keyboard will become low to prevent, via N_1, other keyboards from placing addresses on to the keyboard address bus (see Fig. 58).

The 'key active' signal is passed to all keyboards between the mother board and the keyboard at which the switching takes place via gates N_2 and N_3. If, however, a key with the same number is pressed on a preceding keyboard, this will deactuate the original keyboard, but that does not matter: the address has already been read. The original switching instruction is thus processed before the circuit reacts to the second key impression.

Construction

Since the double-sided PCB (see Fig. 59) is not through-plated, greater accuracy than usual is required in populating the board. A number of through-connexions are made by pins of the ICs. These circuits are therefore not fitted in sockets so that their pins can be soldered at both sides of the board.

Relevant holes may be through-plated conveniently by fitting M3 screws in the fixing holes and then to place the board on the screwheads on a flat surface. The board will then 'float' about 1.5–2 mm above the surface. Fit short lengths of bare wire through the appropriate holes, cut them at equal height above the board surface and solder them to the holes. Reverse the board

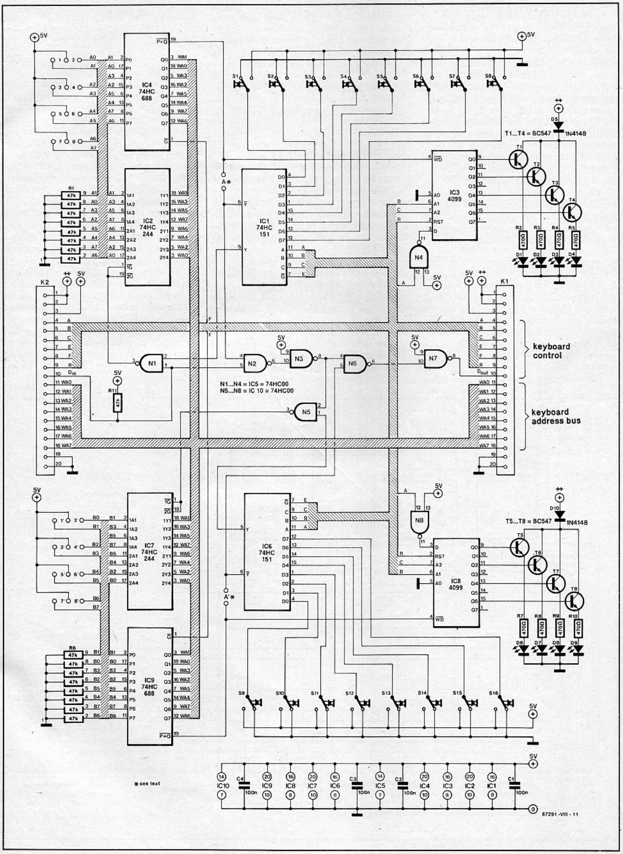


Fig. 57. The diagram shown here consists of two keyboard circuits: one above and one below connectors K_1 and K_2.

and solder the lengths of wire at the other side of the board. Make sure that the through-contacts under the switches are short, otherwise the switches will be seated askew.

Once this preliminary work has been done, the components may be mounted. All of them, except the switches, the LEDs and the jumpers, are soldered at both sides of the board. Note that since R_2–R_5, R_7–R_{10}, T_1–T_8 and the LEDs are to be fitted underneath the switch hoods, they must be mounted before the switches.

Fit the transistors close to the board so that there is no likelihood of their being touched when a switch is pressed.

Resistor arrays R_1 and R_6 may be replaced by vertically mounted discrete resistors (see Fig. 51 – Part 8). The common earth connexion of these resistors is at the underside of the board marked by a dot.

Reducing the cost

If you have no intention of ever controlling the keyboards from the mother board via an RS232 interface, the cost of the present circuit may be reduced by replacing IC_4 and IC_9 by wire links A and A' respectively. Through-contacts must then be made where otherwise the pins of these ICs would be.

Connectors K_1 and K_2 enable a number of keyboards to be connected in parallel: K_1 is then linked by a suitable cable to K_2 on the next keyboard. Connector K_1 on he last (extreme right) keyboard is connected to the mother board.

If the keyboards are intended to be located in a fixed position, for instance, on a control panel, the (fairly expensive) connectors may be replaced by wire links (standard half-inch staples are excellent for this purpose!).

Locating addresses

Since each keyboard can control two decoders, two addresses have to be located on it. These addresses may be placed with the aid of jumpers (wire links). Jumpers 1–8 pertain to the upper keyboard and links 1'–8' to the lower keyboard. Setting the addresses is greatly facilitated with the aid of Table 7.

It is, of course, essential that the addresses on the keyboard and the associated decoder are identical.

If Märklin decoders are used, the number of each jumper in the table is identical with that of the closed contact of the DIL address location switch.

The numbers of the points (turnouts) in the table are important if turnout switching instructions are given via an RS232 interface. Since only 256 turnouts (numbers 0–255) can be controlled via this interface, a number of decoders (shaded in the table) can be controlled only via the keyboards.

Testing

Connect the keyboard to the mother board after making sure that the power supply is not switched on. Verify that jumper A on the mother board is fitted to ensure that the LEDs on the keyboard will be powered.

Switch on the power supply with S_1 on the mother board permanently depressed (this will initiate the service routine as described in Part 8). If IC_4 and IC_9 are used, D_1–D_4 and D_6–D_9 respectively should light alternately in the same rhythm as the yellow LED on the mother board.

Verify that at pin 11 of IC_1 and IC_5 a 1 Hz signal exists; at pin 10 a 0.5 Hz signal and at pin 9 a 0.25 Hz signal.

When the service routine is disabled, all LEDs on the keyboards must go out.

In the stop condition (green LED on the mother board does not light), the keyboard is deactuated. Only when the GO instruction is given via S_1 on the mother board or the RS232 interface will the keyboard be actuated. As long as one of the keys is then depressed, the yellow LED on the mother board should light to indicate that the rele-

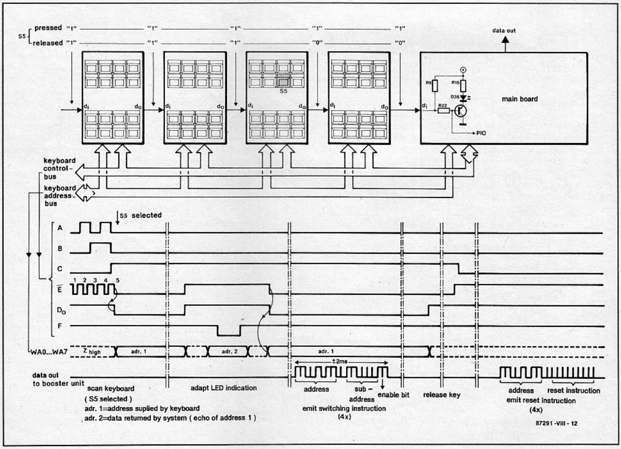


Fig. 58. Timing diagram when a key (here S_5) is pressed. Control takes place from the mother board.

vant decoder output is active. The remainder of the keys can not be operated. When the key is released, the relevant decoder output becomes inactive.

Special cases

In standard form, the keyboard is intended for the control of eight bistable devices containing two solenoids, such as normal turnouts (points) and signals, and also the universal signals and switching decoder described in Part 4 (May 1989), which has four bistable outputs.

Each standard turnout or signal is controlled by two switches and monitored by one (red) LED to indicate its position.

In model railways there are also devices that have an odd number of solenoids, such as sidings or passing loops with only one solenoid, or signals with three positions: stop–go–slow.

The number of switches required on the keyboard is the same as the number of solenoids to be controlled. Therefore, a three-position signal is controlled by S_1, S_2 and S_4; S_3 is then not used and, for safety's sake, better not fitted. If two sidings or passing loops are controlled by, say, S_5 and S_6, the associated LED (D_3) is better not fitted (to obviate the thought that there is a connection between the two).

Parts list

Resistors:
R_1;R_6 = SIL array 8×47k
R_2–R_5;R_7–R_{10} = 470Ω
R_{11} = 47k

Capacitors:
C_1–C_4 = 100n

Semiconductors:
D_1–D_4;D_6–D_9 = LED (in keyboard switch)
D_5;D_{10} = 1N4148
T_1–T_8 = BC547
IC_1;IC_6 = 74HC151
IC_2;IC_7 = 74HC244
IC_3;IC_8 = 4099
IC_4;IC_9 = 74HC688
IC_5;IC_{10} = 74HC00

Miscellaneous:
K_1 = 20-way SIL PCB header, angled.
K_2 = 20-way SIL PCB socket, angled.
S_1;S_3;S_5;S_7;S_9;S_{11};S_{13};S_{15} = ITW dataswitch (series 61) with wide keycap, Type 61-10204000 *.
S_2;S_4;S_6;S_8;S_{10};S_{12};S_{14};S_{16} = ITW dataswitch with wide keycap and integral LED, Type 61-10404010 *.
Qty. 8: 3-way pin headers (0.1-inch raster) and max. 8 jumpers for keyboard programming.
PCB Type 87291-7

Parallel control

If the same address is located on two different keyboards, the boards are electrically coupled. If on one of them a switch is operated, the LEDs on the other will react (provided that IC_4 and IC_9 are used).

If the track has a small marshalling yard far away from the main control centre, it may be useful to give that yard a local control unit in parallel with the central control panel. For this, a keyboard with the same address as set at the central control may be used. It should be placed close to the yard and be connected to K_2 of the extreme left-hand keyboard via an 18-way (preferably flat) cable (18-way is sufficient since only single earth and ++ supply lines are needed).

Track layout on control panel

Even in model railway systems, ergonomics take on a more and more prominent role. For instance, if the track is extensive, the operating switches are nowadays often located on the central control panel in positions that correspond with the actual

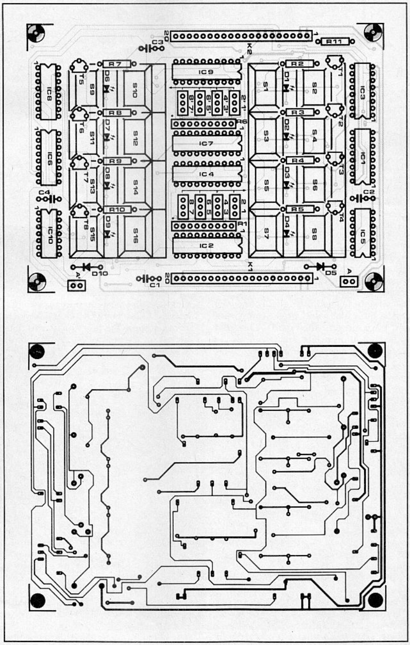


Fig. 59. The printed-circuit board has provision for building two keyboards.

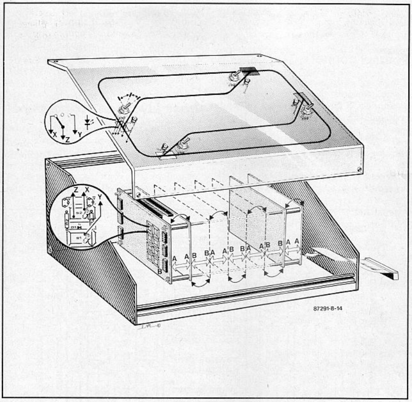


Fig. 60. Artist's impression of the control unit with a track layout provided on its front panel.

track layout. This may also be done in the present system. The PCBs for the keyboards are then housed somewhere under the control panel. If many keyboards are used, it is advisable to fit them as sandwiches as shown in Fig. 60. In that case, use straight instead of angled connectors and fit these alternately on the component and track sides of the boards. Threaded rods and appropriate spacers give the whole sufficient mechanical rigidity.

Switches and LEDs are connected to the PCBs with discrete wires. If switches with spring-loaded make contacts are used (as opposed to the change-over contacts on the original switches), pull-down resistors as shown in Fig. 60 are needed. Better are spring-loaded 3-position miniature toggle switches. These have two make contacts and can assume the function of two data switches for the control of one turnout or one signal.

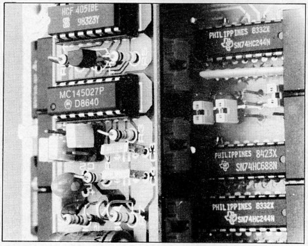


Fig. 61. The jumper patterns on the keyboard and decoder board must be identical.

keyboard decoder	no. of points	jumpers required
0	0...3	- - - - - - - -
1	4...7	- 2 3 - 5 - 7 -
2	8...11	- - 3 - 5 - 7 -
3	12...15	1 - - 4 5 - 7 -
4	16...19	- 2 - 4 5 - 7 -
5	20...23	- - - 4 5 - 7 -
6	24...27	1 - - - 5 - 7 -
7	28...31	- 2 - - 5 - 7 -
8	32...35	- - - - 5 - 7 -
9	36...39	1 - 3 - - 6 7 -
10	40...43	- 2 3 - - 6 7 -
11	44...47	- - 3 - - 6 7 -
12	48...51	1 - - 4 - 6 7 -
13	52...55	- 2 - 4 - 6 7 -
14	56...59	- - - 4 - 6 7 -
15	60...63	1 - - - - 6 7 -
16	64...67	- 2 - - - 6 7 -
17	68...71	- - - - - 6 7 -
18	72...75	1 - 3 - - - 7 -
19	76...79	- 2 3 - - - 7 -
20	80...83	- - 3 - - - 7 -
21	84...87	1 - - 4 - - 7 -
22	88...91	- 2 - 4 - - 7 -
23	92...95	- - - 4 - - 7 -
24	96...99	1 - - - - - 7 -
25	100...103	- 2 - - - - 7 -
26	104...107	- - - - - - 7 -
27	108...111	1 - 3 - 5 - - 8
28	112...115	- 2 3 - 5 - - 8
29	116...119	- - 3 - 5 - - 8
30	120...123	1 - - 4 5 - - 8
31	124...127	- 2 - 4 5 - - 8
32	128...131	- - - 4 5 - - 8
33	132...135	1 - - - 5 - - 8
34	136...139	- 2 - - 5 - - 8
35	140...143	- - - - 5 - - 8
36	144...147	1 - 3 - - 6 - 8
37	148...151	- 2 3 - - 6 - 8
38	152...155	- - 3 - - 6 - 8
39	156...159	1 - - 4 - 6 - 8
40	160...163	- 2 - 4 - 6 - 8
41	164...167	- - - 4 - 6 - 8
42	168...171	1 - - - - 6 - 8
43	172...175	- 2 - - - 6 - 8
44	176...181	- - - - - 6 - 8
45	180...183	1 - 3 - - - - 8
46	184...187	- 2 3 - - - - 8
47	188...191	- - 3 - - - - 8
48	192...195	1 - - 4 - - - 8
49	196...199	- 2 - 4 - - - 8
50	200...203	- - - 4 - - - 8
51	204...207	1 - - - - - - 8
52	208...211	- 2 - - - - - 8
53	212...215	- - - - - - - 8
54	216...219	1 - 3 - 5 - - -
55	220...223	- 2 3 - 5 - - -
56	224...227	- - 3 - 5 - - -
57	228...231	1 - - 4 5 - - -
58	232...235	- 2 - 4 5 - - -
59	236...239	- - - 4 5 - - -
60	240...243	1 - - - 5 - - -
61	244...247	- 2 - - 5 - - -
62	248...251	- - - - 5 - - -
63	252...255	1 - 3 - - 6 - -
64	256...259	- 2 3 - - 6 - -
65	260...263	- - 3 - - 6 - -
66	264...267	1 - - 4 - 6 - -
67	268...271	- 2 - 4 - 6 - -
68	272...275	- - - 4 - 6 - -
69	276...279	1 - - - - 6 - -
70	280...283	- 2 - - - 6 - -
71	284...287	- - - - - 6 - -
72	288...291	1 - 3 - - - - -
73	292...295	- 2 3 - - - - -
74	296...299	- - 3 - - - - -
75	300...303	1 - - 4 - - - -
76	304...307	- 2 - 4 - - - -
77	308...311	- - - 4 - - - -
78	312...315	1 - - - - - - -
79	316...319	- 2 - - - - - -
80	320...323	1 - 3 - 5 - 7 -

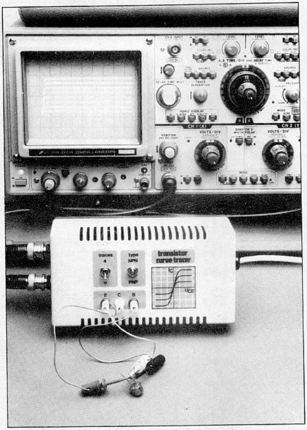
Table 7. Up to 256 turnouts or signals (numbers 0–255) may be controlled via an RS232 interface; the remainder (shaded portion) can be controlled only via the keyboards.

TRANSISTOR CURVE TRACER

T. Wigmore

With so many transistors used in today's equipment, a good tester for these devices is a must in every electronics workshop. And yet, most of us use a multimeter to check transistors. Although such a test is usually adequate for a quick o.k./faulty test, it fails to provide information on the characteristics of the device under test. The curve tracer presented here works in conjunction with an oscilloscope, and is capable of performing a stepped current amplification test on pnp as well as on npn transistors. The instrument so allows unknown or unmarked types to be matched to known ones, which is a frequent requirement in fault-finding and repair work.

The so-called output curve is among the most important transistor characteristics. The curve shows how the collector current (on the *Y*-axis) depends on the collector-emitter voltage (on the *X*-axis), with base current for the relevant bias setting as a parameter. By stepping up the base current within the permissible range, characteristic curves of different edge steepness are obtained on an oscilloscope or plotter. These curves indicate whether the transistor is good or faulty, and also allow its current amplification to be estimated. Furthermore, a useful indication is provided of the linearity and the resistance characteristic in the saturation range. Finally, since the tester can handle both npn and pnp transistors, the curves allow matching, complementary devices to be selected from available batches.



Digital and analogue

Two quite different test signals are required to write the output characteristic of a transistor: the base current must be switched in steps, while the collector voltage must have a continuous range of 0 V to the maximum value. Not surprisingly, therefore, the base current is controlled digitally, and the collector voltage by an analogue circuit. The latter also has a controlling function on the base current generator to prevent this stepping up or down while a curve is being written.

The collector voltage is supplied by a triangular generator consisting of a Schmitt-trigger and an integrator (see Fig. 1). The Schmitt-trigger is composed of a 1.45-times amplifier and a comparator. The amplifier supplies the reference level for the comparator. To ensure the required thresholds and hysteresis, the reference level, in turn, depends on the output level of the Schmitt-trigger. Diodes between the amplifier and the comparator allow the two switching thresholds of the Schmitt-trigger to be set to 0 V and 8 V, or 0 V and −8 V, as required for npn or pnp transistors respectively. The combination of the Schmitt-trigger and the integrator results in a triangular-wave generator whose output voltage varies between 0 V and 8 V, or 0 V and −8 V. This signal is used as the collector-emitter voltage for the transistor under test.

The triangular signal is fairly simple to convert into a rectangular one, which is used to clock the digital part of the circuit. As the collector-emitter voltage starts to rise (from 0 V with npn transistors, and from −8 V with pnp types), a counter, and with it the base current, is incremented by one step. The counter drives a discrete digital-to-analogue (D-A) converter that translates the 3-bit counter value into base current steps of 25 μA. Switch S_2 allows the D-A converter to be driven by two instead of three bits to select between four or eight displayed characteristic curves.

Although in theory not quite correct for the relevant test on the transistor, an emitter resistor is used to translate current into voltage. This arrangement was preferred over a collector resistor because most oscilloscope inputs have one grounded terminal.

Finally, a current limiter has been added on the integrator output stage to eliminate the risk of the test circuit being overloaded by a faulty transistor.

Detailed operation

The power supply — see the circuit diagram of Fig. 2 — inclusive of the mains transformer is accommodated on the printed-circuit board. The secondary transformer voltage is rectified to give a symmetrical direct voltage. Under 'no-load conditions, there is about 14 V on C_2 and C_3. Since single-phase rectification is used, the supply voltage has a relatively high ripple, and falls a few volts when a good transistor with high current amplification is being tested. Under this condi-

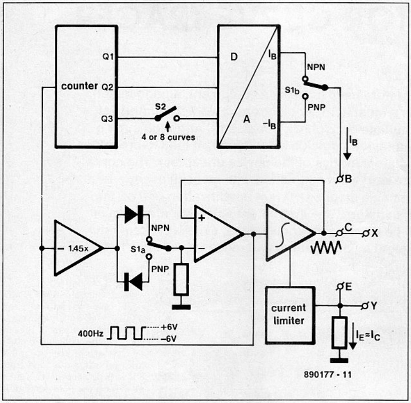


Fig. 1. **Block diagram of the transistor curve tracer.**

counter state	4 curves		8 curves	
	pnp	npn	pnp	npn
000	−75	0	−175	0
001	−50	25	−150	25
010	−25	50	−125	50
011	0	75	−100	75
100	−75	0	−75	100
101	−50	25	−50	125
110	−25	50	−25	150
111	0	75	0	175
	base current I_B (μA)			

Table 1. Digital current control.

tion, the transformer's secondary voltage will also drop to its nominal (loaded secondary) value. The unregulated supply voltage is used to power the analogue part of the circuit. This voltage is too high to power counter IC$_1$. Also, the supply voltage of the counter must be regulated because it determines the base current for the transistor under test. Zener diodes are, therefore, used to stabilize the IC supply voltage at ±5.6 V. The symmetrical supply enables the counter outputs to switch between positive and negative voltages relative to ground, corresponding to a logic 1 and a logic 0 respectively. These

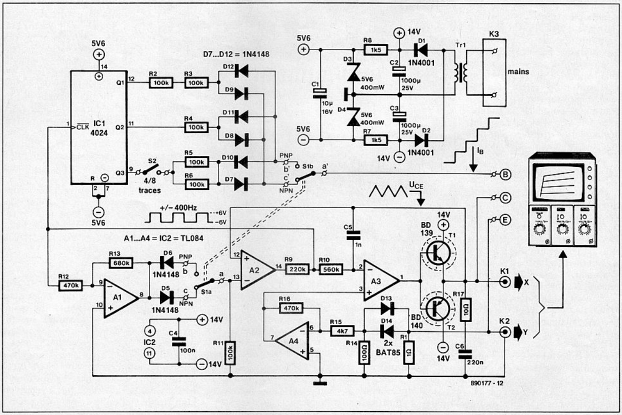


Fig. 2. **Circuit diagram of the curve tracer, which is a combination of analogue and digital electronics.**

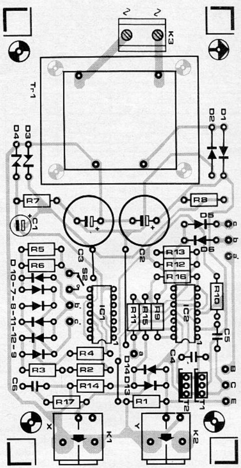


Fig. 3. Component mounting plan of the single-sided printed-circuit board for the transistor curve tracer.

Parts list

Resistors:
R_1 = 1Ω0
R_2 – R_6;R_{11} = 100k
R_7;R_8 = 1k5
R_9 = 220k
R_{10} = 560k
R_{12};R_{16} = 470k
R_{13} = 680k
R_{14} = 100Ω
R_{15} = 4k7
R_{17} = 10Ω

Capacitors:
C_1 = 10μ; 16 V; radial
C_2;C_3 = 1000μ; 25 V; radial
C_4 = 100n
C_5 = 1n0
C_6 = 220n

Semiconductors:
D_1;D_2 = 1N4001
D_3;D_4= zener diode 5V6; 400 mW
D_5 – D_{12} = 1N4148
D_{13};D_{14} = BAT85
T_1 = BD139
T_2 = BD140
IC_1 = 4024
IC_2 = TL084

Miscellaneous:
S_1 = miniature double-pole toggle (DPDT) switch.
S_2 = miniature on/off (SPST) switch.
Tr_1 = PCB mount transformer 9 V @ 7.5VA.
K_1;K_2 = BNC socket (e.g. PCB-mount type UG-1094/UP from Monacor).
K_3 = 2-way screw terminal block, pitch 10 mm.
Heat-sinks for T_1 and T_2.
Enclosure 150×80×50 mm, e.g. Bopla type E440VL.
PCB Type 890177 [redacted]

levels enable the D-A converter to be kept simple but still capable of generating the required positive and negative base currents.

The D-A converter consists of resistors R_2–R_6 and diodes D_7–D_{12}. The latter parts separate the positive and negative half periods of the currents that may be carried by the resistors. The value and direction (sign) of the currents depend on the counter value, and the positions of S_1 and S_2, which are in accordance with the transistor type. Table 1 summarizes all conditions that apply when a transistor is connected for testing.

The analogue part of the circuit closely follows the block diagram. What is not so apparent, however, is how the operation of the analogue circuit remains largely unaffected by the unregulated supply voltage. For opamp A_1, this is relatively easy to understand because the output voltage of this amplifier simply follows the input voltage with practically no effect of the supply voltage. This is not so with comparator A_2, since here the input voltage determines how the output voltage shifts as far as possible towards one of the supply voltages, which are subject to considerable variation. Clearly, if a fluctuating input voltage were applied to the integrator around A_3, the circuit would be incapable of generating a well-defined triangular output voltage. Note that this, in principle, need not be a problem: the only requirement is that the output voltage swings between two extremes.

The comparator, however, serves to clock the counter, which has a lower supply voltage. Clamping diodes are connected to the clock input of the counter as a protection against too high voltages. Together with current limiter R_9, the diodes ensure a stable rectangular voltage of about 6 V_{pp} at the input of the counter and, therefore, at the input of the integrator. The result of the clamping and regulation circuit is a triangular output voltage whose rate of rise is practically independent of the supply voltage.

The stabilized rectangular voltage also enables A_1 to supply a reference level for comparator A_2 that is hardly affected by the supply voltage. Hence, the inflection points of the triangular voltage occur at accurately defined and stable voltage levels.

In order to be able to test medium- and high-power transistors also, the integrator opamp is followed by two transistors that are protected against short-circuits by the circuit around D_{13}, D_{14} and A_4. The two Schottky diodes type BAT85 have a threshold voltage of about 0.4 V. They conduct when the voltage on R_1 (I_c>400 mA) exceeds the threshold, and cause A_4 to shift the voltage at the + input of integrator A_3 to a level where the integration operation stops. The + input is

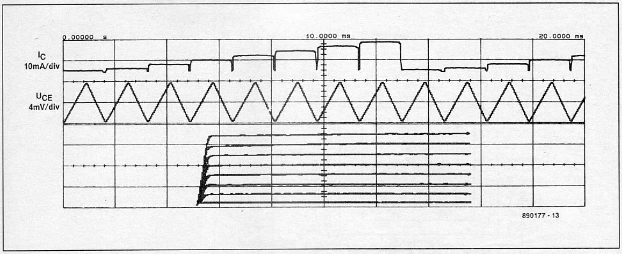


Fig. 4. Screendump provided by a Hewlett-Packard digital oscilloscope to illustrate the operation of the transistor curve tracer.

normally at 0 V. When actuated, the protection circuit causes the oscilloscope to show only a fixed bright spot instead of four or eight traces.

Building the tracer

The complete circuit is accommodated on the printed-circuit board shown in Fig. 3. Populating the board is straightforward and should not cause any difficulty.

The enclosure stated in the parts list requires the four squares at the corners of the PCB to be cut off. Great attention should be paid to safety as the mains voltage is applied direct to the board via a 2-way screw terminal block.

Although the board is designed to accommodate PCB-mount BNC sockets, standard types may also be used with short lengths of screened wire. Connect switch S_1 to terminals a, b, c, a', b' and c', which are at different locations on the board. Be sure not to mix up points a and a'.

Use short, flexible wires terminated in small crocodile clips to connect the transistor to the tester. Do not make these flying leads longer than about 10 cm on penalty of creating stray capacitance that may affect the test results.

Finally, insert a small rubber cabinet foot between the facing metal tabs of T_1 and T_2 to eliminate any risk of a short-circuit.

Using the curve tracer

Before discussing the practical use of the transistor curve tracer, it is worth while to have a look at Fig. 4. This shows the printout on paper (screendump) obtained with a Hewlett-Packard digital oscilloscope and associated plotter. The signals on the upper two traces, I_c and U_{c-e}, are combined with the aid of the *X-Y* mode of the oscilloscope. The resulting graphs form the output characteristics of the transistor under test. It should be noted that each graph is written two times: first with U_{c-e} rising, and then with U_{c-e} falling. This results in the 'chopped' upper I_c curve. The output characteristics were obtained with a transistor Type BC141-10.

Connect the curve tracer to the oscilloscope via two short coax cables. Initially, set the scope to *X-Y* mode, 10 mV/div. on the *Y* channel, and 1 V/div. on the *X* channel. Since the collector current is measured via a 1 Ω resistor, the *Y*-axis indicates the voltage in volts and the current in ampères, obviating calculations. For pnp transistors, the characteristic must be inverted. This is achieved with the INVERT control provided on most oscilloscopes.

The photographs of Fig. 5 show a few transistor characteristics obtained with the curve tracer. Figure 5a shows the characteristic of a BC547A. By comparison, a BC547B (Fig. 5b) has a higher current amplification, but a quite different rate of rise of the top three curves. The curves in Fig. 5c belong to a BC550, and are even straighter than those in Fig. 5b, indicating better linearity than the previous two transistors. In addition, the BC550 has very little noise, which makes it eminent for application as and audio preamplifier.

Care should be taken when testing a high current gain transistor such as the BC550C (Fig. 5d). The current amplification is so high that there exists a real danger of the maximum permissible collector current or dissipation being exceeded (note that three of the eight curves run off the oscilloscope screen). If necessary, use S_2 to reduce the number of curves from eight to four. This setting also reduces the maximum base current from 175 µA to a safer 75 µA.

The curve tracer is also fine for selecting a replacement type for an unknown transistor that has been found to be faulty. Fortunately, much consumer equipment has a number of identical transistors. Remove one with the same type number as the faulty transistor, and connect it to the curve tracer. The resulting characteristic on the scope will, in many cases, enable you to find a near equivalent transistor of known type and make from an available lot.

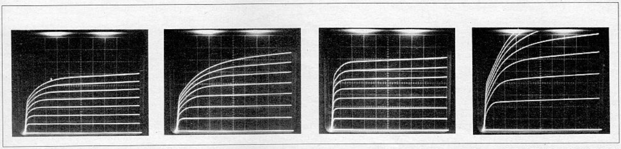


Fig. 5. Examples of curves obtained with some commonly used transistors. From the left to the right: BC547A, BC547B, BC550, BC550C.

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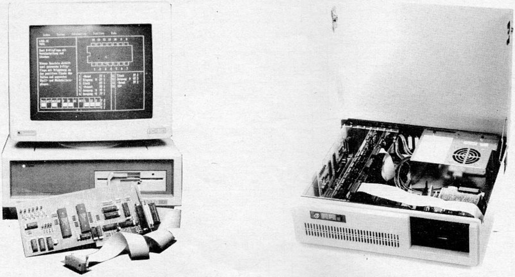
INTEGRATED-CIRCUIT TESTER



This IC tester, designed by ELV GmbH, comes as an insertion card for IBM PC-XT/AT and compatibles. The card and the associated ZIF socket allow logic function tests to be carried out on a wide range of CMOS and TTL integrated circuits housed in DIL packages with up to 20 pins. The article also describes the menu-driven control program for the IC tester, which makes use of a user-definable library to test over 500 standard components.

It is often necessary to check the operation of standard ICs, whether these are new or used. Testing small-scale integration (SSI) circuits with relatively few gates can be done without too much trouble. However, as the ICs become more complex, checking them with the aid of simple tools such as switches and LEDs becomes much more difficult. In such cases, the IC in question must be removed from the circuit for a separate test, which can be very time-consuming as its pinning and operation have to be studied in detail to arrive at a suitabe test procedure.

This IC tester has been developed to enable rapid and simple functional tests to be carried out on these standard components.

Nearly all components in the standard TTL and CMOS range, up to 20-pin DIL package size, can be tested. Integrated circuits to be tested are simply inserted into the 20-pin ZIF (zero-insertion force) test socket. The notchless short side of the IC is always aligned with pins 10 and 11 of the test socket. Any remaining pins of the socket are not used.

The test system is also suitable for the related LS, HC and HCT families. Only voltage-controlled oscillators (VCOs) and PLL devices such as the CD4046, the 74624, and others can not be tested.

These parts would have increased the complexity of the tester considerably as they require several supply voltages and analogue input signals.

A special multiplexer circuit is used in the tester to check monostable multivibrators. This connects the required resistors and capacitors for the time constants to the appropriate pins.

The IC tester thoroughly checks the logic behaviour of the components under test, and provides an almost instant good/faulty indication on the computer screen. The signal or voltage on any ZIF socket pin depends on the IC to be tested. The possibilities are

- supply voltage +5 V
- supply voltage ground
- logic output 'H' or 'L'
- open collector output

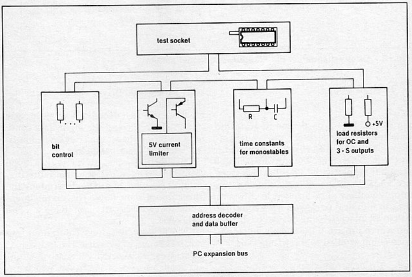

test socket
bit control
5V current limiter
R
C
time constants for monostables
+5V
load resistors for OC and 3-S outputs
address decoder and data buffer
PC expansion bus

Fig. 1. Block diagram of the integrated-circuit tester.

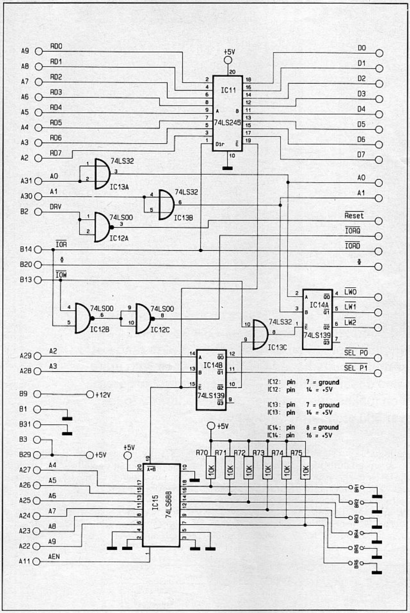


Fig. 2. Circuit diagram of the PC address decoder section.

Signal name	Pin designation track side	Pin designation component side	Signal name
GND	B01	A01	$\overline{\text{I/O CHCK}}$
RESET	B02	A02	D7
+5V	B03	A03	D6
IRQ2	B04	A04	D5
−5V	B05	A05	D4
DREQ2	B06	A06	D3
+12V	B07	A07	D2
reserved	B08	A08	D1
+12V	B09	A09	D0
GND	B10	A10	I/O CHRDY
$\overline{\text{MEMW}}$	B11	A11	AEN
$\overline{\text{MEMR}}$	B12	A12	A19
$\overline{\text{IOWC}}$	B13	A13	A18
$\overline{\text{IORC}}$	B14	A14	A17
$\overline{\text{DACK3}}$	B15	A15	A16
DREQ3	B16	A16	A15
$\overline{\text{DACK1}}$	B17	A17	A14
DREQ1	B18	A18	A13
$\overline{\text{DACK0}}$	B19	A19	A12
CLK	B20	A20	A11
IRQ7	B21	A21	A10
IRQ6	B22	A22	A9
IRQ5	B23	A23	A8
IRQ4	B24	A24	A7
IRQ3	B25	A25	A6
$\overline{\text{DACK2}}$	B26	A26	A5
TC	B27	A27	A6
ALE	B28	A28	A3
+5V	B29	A29	A2
OSC	B30	A30	A1
GND	B31	A31	A0

Table 1. PC expansion slot pinning.

- three-state output
- data or control input

On selection of a particular IC from the data library, the necesary pin configuration conditions are set up automatically by the IC tester. Since the software can not search for a particular IC if the user does not know its name, it is possible for the supply voltage to be applied to different pins in identical packages. This could result in an intact IC being destroyed during the search process if the supply voltage is correct but applied to the wrong pins.

The circuit

The circuit consists of two parts. Figure 2 shows the complete address decoder and Fig. 3 the actual driver circuit for the ICs to be tested.

The address decoder has two basic functions: buffering the eight data lines, and selecting the storage device and buffer, which is described below.

Bidirectional bus driver IC$_{11}$, a Type 74LS245, takes care of the data buffering, while I/O read line $\overline{\text{IOR}}$ determines the direction of data flow. The driver is enabled by address decoder IC$_{15}$, a Type 74LS688.

The IC tester requires a continuous I/O address range of 16 bytes. The individual addresses are selected via A0 to A3, and the main address by A4 to A9, which are fed to the comparator IC$_{15}$. The address range can be preset by wire links Br$_1$ to Br$_6$.

When the main address is sent by the CPU in the PC, a low level appears at output pin 19 of 8-bit comparator IC$_{15}$. Depending on the state of address lines A2 and A3 of the PC bus, one of the four outputs of IC$_{14B}$, $\overline{\text{Q0}}$ to $\overline{\text{Q3}}$, goes low. Outputs $\overline{\text{Q0}}$ and $\overline{\text{Q1}}$ then select either one of two PIOs (parallel input/output) devices IC$_1$ or IC$_2$. Output $\overline{\text{Q2}}$ of IC$_{14B}$, together with I/O write line $\overline{\text{IOW}}$, enables IC$_{14A}$, a 74LS139, via OR gate IC$_{13C}$. Outputs $\overline{\text{Q0}}$, $\overline{\text{Q1}}$ and $\overline{\text{Q2}}$ then clock data into the appropriate latch, IC$_8$, IC$_9$ or IC$_{10}$.

Address lines A0 and A1 are buffered by OR gates IC$_{13A}$ and IC$_{13B}$. The reset signal, DRV, is inverted by IC$_{12A}$ before it is fed to the $\overline{\text{M1}}$ inputs of PIOs IC$_1$ and IC$_2$. NAND gates IC$_{12B}$ and IC$_{12C}$ combine I/O write and read lines $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ to pro-

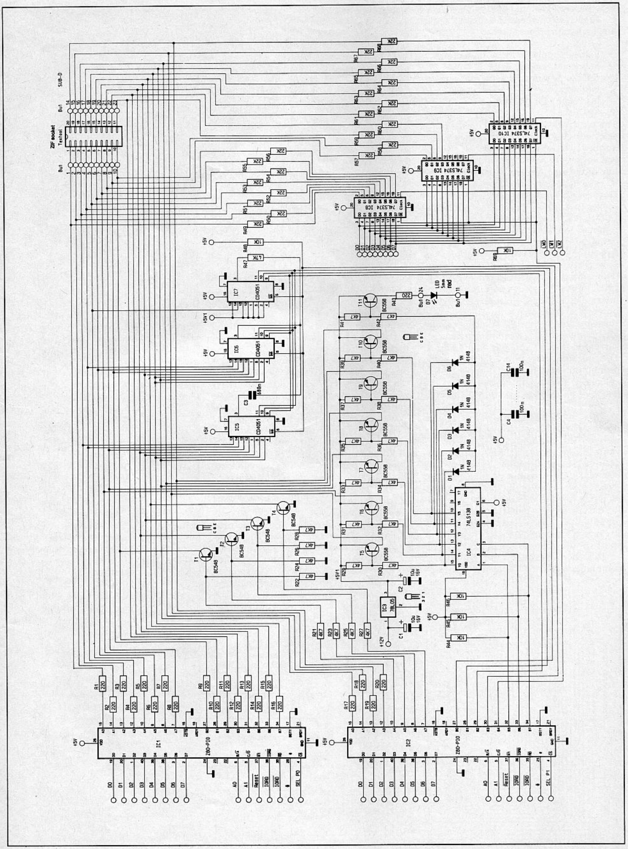


Fig. 3. This section of the circuit performs the actual testing of logic integrated circuits.

vide I/O access signal $\overline{IORQ}$.

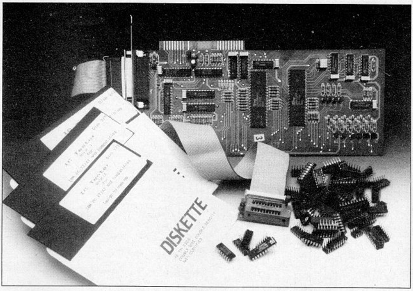
The IC tester consists of several, separate, logic units. These are:

- voltage supply for the IC under test
- logic condition simulator
- *R-C* combination for monostable multivibrators
- load circuit for the drivers

The positive supply voltage for the ICs is selected with the aid of decoder IC$_4$, and applied the appropriate pins on the ZIF test socket via R$_{29}$ to R$_{40}$, and T$_5$ to T$_{10}$. If one of the six supply voltage lines for the IC is switched on, one of the diodes D$_1$ to D$_6$ causes the red LED adjacent to the test socket to light via buffer T$_{11}$. While this LED lights, the IC to be tested must not be removed or inserted to avoid it being damaged by voltage transients. The positive supply voltage (+5.1 V) is supplied by voltage regulator IC$_3$, an 78L05. The regulator is a safety measure against short circuits in the IC under test causing the internal 5 V supply voltage of the computer to break down with all the costly consequences for the PC. Voltage regulator IC$_3$ limits the maximum short-circuit current to a safe value of about 100 mA. The negative supply voltage, i.e., the ground potential for the IC under test, is connected to the appropriate pin of the test socket via one of four transistors T$_1$ to T$_4$.

The two Z80-PIOs, IC$_1$ and IC$_2$, form the heart of the circuit. These ICs from the well-known Z80 family have the great advantage that their I/O lines are bit-programmable to function as inputs or outputs. In this way it is possible to have, for example, pin 1 on the test function as an input, pin 2 as an output. etc. Obviously, this is an indispensable requirement for an IC tester. Current limiting resistors R$_1$ to R$_{20}$ protect the PIOs in case of a short-circuit when testing ICs.

To test monostables, the required *R-C* combinations can be connected to the appropriate pins of the device under test. This is achieved with the aid of analogue multiplexers Type CD4051 in positions IC$_5$, IC$_6$ and IC$_7$. The values of C$_3$ and R$_{47}$ define the time constants, and have been chosen to enable a great many monostables to be checked. The *R-C* combination can be switched on with control line $\overline{INH}$, which is connected to pin 6 of all three multiplexers. The binary code on the three channel selection inputs, pins 9, 10 and 11, allows one of seven connection modes for the *R-C* combination to be used.



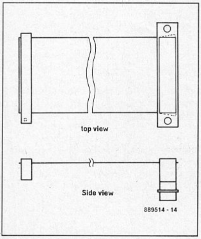


Fig. 4. **Flat-ribbon cable construction.**

When testing open-collector (OC) and three-state outputs, it is necessary to load these with a high-value resistor. The outputs of latches IC$_8$, IC$_9$ and IC$_{10}$ are controlled by the logic level at pin 1 ($\overline{OE}$; output enable). If $\overline{OE}$ is low, the 20 outputs of IC$_8$, IC$_9$ and IC$_{10}$ supply the previously latched data word. The logic levels that form the dataword are fed to the corresponding pins of the test socket via load resistors R$_{49}$ to R$_{68}$. The 'response' of the IC under test to the applied test levels is then transferred to the control software via R$_1$ to R$_{20}$ and the inputs of the two PIO circuits.

Control software

The extensive control program supplied with the kit is menu-driven and has a number of data libraries. The program is supplied on a 5¼-inch 360 Kbyte floppy disk. The README.IC file, found on it gives a complete description of the program and explains how to install it into a hard disk. Hard copy of this file is conveniently obtained by entering

```
COPY README.IC LPT 1:<CR>
```

The complete test software is menu-guided and therefore easy to operate. To start the program, enter

```
ICTEST <CR>
```

The instructions on the screen are self-explanatory. A help function is available at any time by pressing function key F1. The software is compatible with Monochrome (MDA), Hercules and EGA video cards, which are automatically recognized during initialization.

The I/O base address for the IC tester is normally at 300$_H$. If the card is to occupy another range, the program must be started with

```
ICTEST <address> <CR>
```

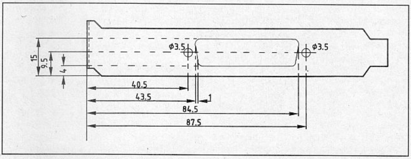


Fig. 5. **Cutting and drilling details of the support bracket at the rear side of the PC card.**

where <address> is entered in hexadecimal.

The software package is capable of selecting and testing over 500 IC types. In addition, ICs which are not included in

I/O Address	Function
000H–00FH	DMA-Controller (8237A-5)
020H–021H	Interrupt-Controller (8259-5)
040H–043H	Timer/Counter (8253-5)
060H–063H	System Register (8255A-5)
080H–083H	DMA-Side Register (74LS670)
0A0H–0BFH	NMI-Interrupt Register
0C0H–0FFH	Reserved
100H–1FFH	Front Panel Controller
200H–20FH	For Computer Games (Game Port)
210H–217H	Additional Unit
220H–24FH	Reserved
278H–27FH	Second Printer
2F8H–2FFH	Second Serial Interface
300H–31FH	Prototype Card
320H–32FH	Hard Disk-Controller
378H–37FH	Printer Interface (parallel)
380H–38FH	SDLC-Interface
3A0H–3AFH	Reserved
3B0H–3BFH	Monochrome Adaptor and printer
3C0H–3CFH	Reserved
3D0H–3DFH	Colour Graphics Card
3E0H–3E7H	Reserved
3F0H–3F7H	Floppy Controller
3F8H–3FFH	Serial Interface

Table 2. PC I/O address assignment.

Base address	I/O Component
+ 0	PIO 1 Port A Data
+ 1	PIO 1 Port B Data
+ 2	PIO 1 Port A Control
+ 3	PIO 1 Port B Control
+ 4	PIO 2 Port A Data
+ 5	PIO 2 Port B Data
+ 6	PIO 2 Port A Control
+ 7	PIO 2 Port B Control
+ 8	Latch 0 Load Pin 1 – 8
+ 9	Latch 1 Load Pin 9 – 12
+ A	Latch 2 Load Pin 13 – 20
+ B	
+ C	
+ D	
+ E	
+ F	

Table 3. Address map of the IC tester.

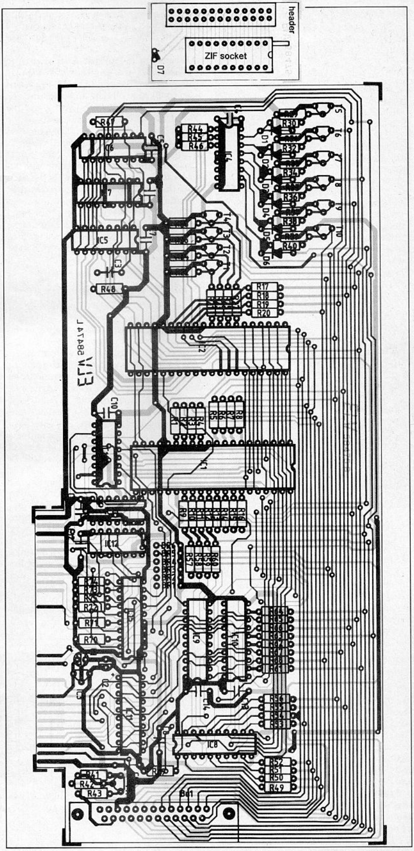


Fig. 6. Component mounting plans of the main board and the test socket board.

Parts list

Resistors:
$R_1 - R_{20}; R_{43} = 220\Omega$
$R_{21} - R_{42} = 4k7$
$R_{44}; R_{45}; R_{46}; R_{48}; R_{69} - R_{75} = 10k$
$R_{49} - R_{68} = 22k$
$R_{47} = 47k$

Capacitors:
$C_4 - C_{14} = 100n$
C3 = 680n
$C_1; C_2 = 10\mu; 16V$

Semiconductors:
$IC_1; IC_2$ = Z80PIO
$IC_5 - IC_7$ = CD4051
IC_{12} = 74LS00
IC_{13} = 74LS32
IC_4 = 74LS138
IC_{14} = 74LS139
IC_{11} = 74LS245
$IC_8 - IC_{10}$ = 74LS374
IC_{15} = 74LS688
IC3 = 78L05
$T_1 - T_4$ = BC548
$T_5 - T_{11}$ = BC558
$D1 - D_6$ = 1N4148
D_7 = LED (5 mm, red)

Miscellaneous:
20-way ZIF test socket.
26-way straight PCB header (double-row).
26-way IDC socket.
25-way sub-D plug for cable mounting.
25-way sub-D socket for PCB edge mounting.
25-way flat-ribbon cable, length approx. 50 cm.
PCB mounting panel for PC.

the standard library may be added at a later stage. How the user can accomplish this is explained at length in the file README.IC.

The software will also function without the associated IC test card being inserted. This means that the program may serve as a reference to look up IC pin-outs, because a connection picture appears on the screen for every IC that can be tested.

Construction

The IC tester consists of two printed circuit boards, which are connected via a 25-way flat ribbon cable. The main control circuit is accommodated on a double-sided, through-plated PCB .(size: 235×110 mm). A 25-way sub-D socket on the back panel bracket provides the connection to the auxiliary PCB (size: 46×24 mm), which accommodates the 20-way ZIF socket.

Both PCBs are populated in the normal way. Refer to the parts list and the board layout when fitting the passive and then the active components on to the PCB. As all components are accommodated on the two PCBs, assembly is relatively simple. Care should be taken to mount the components at the lowest possible height to avoid contact with the PCB in the adjacent PC slot. Sockets are, therefore, not used for the ICs.

There are only three components on the smaller board: pin header St_1, 20-way Textool socket Sk_1 and LED D7. The board is so small as to obviate an enclosure.

Clamp the 25-pin sub-D plug and the 26-pin IDC socket on to the ends of the flat-ribbon cable (Fig. 4). The coloured wire at one side of the flat-ribbon cable is at the side of pin 1, both of the sub-D connector and the IDC connector. The latter has one non-used pin, and is plugged on to the header with the coloured wire at the side of the socket lever.

One of the empty PCB support brackets on the rear panel of the computer is removed and cut as shown in Fig. 5 to enable the 25-way socket on the PCB to be fitted.

Address selection

Solder the I/O address wires in place before taking the board into operation. Table 2 gives a detailed description of the available I/O address range.

In order to explain the setting of the I/O address decoder, which consists of Br_1 to Br_6, address 300_H is considered the base address for the IC tester. As the system requires a continuous I/O address range of 16 bytes, the I/O base address need be decoded only once. Since the base address is a multiple of 16, its last address digit is always 0. The first digit of the I/O address can not be higher than 3, as the 16 bit I/O address range of the IBM-PC is decoded with 10 bits only, corresponding to a maximum of 400_H. This 3 is set in binary form by means of wire links Br_5 and Br_6. The second digit can take a value between O and F, and is set as a binary code using Br_1 to Br_4.

For I/O base address 300_H, wire links Br_1 to Br_4 must be installed (3), while Br_5 and Br_6 remain open (00). Table 3 shows the distribution of the 16 I/O addresses over the components on the IC tester card.

After carefully checking the construction a second time, the IC tester is ready to be taken into operation.

Practical use

After inserting the card into the appropriate slot in the PC, connect the small PCB with the flat-ribbon cable, and close the case of the PC. Switch on the computer and wait for its normal initialization to complete. Load and start the control program for the IC tester by selecting the appropriate floppy disk drive and typing

```
ICTEST <CR>
```

Every IC to be tested must be inserted such that its notch is to the side of the lever on the test socket. If the IC has less than 20 pins, it is inserted as shown in Fig. 7.

The software consists of various modules. The actual program is an interpreter, which reads the pin configurations and test conditions of individual ICs from a number of data files. The user is, therefore, in a position to add new ICs as they become available. The library editing functions can be accomplished with almost any word processor as explained in the README.IC file. To shorten the loading time of the disk, the complete program should be transferred to and started from the hard disk. The program, menus and documentation files are in English.

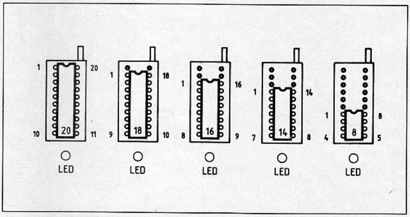


Fig. 7. ICs to be tested must always be plugged into the ZIF socket as shown here.

8098 EVALUATION BOARD

CONSTRUCTION & TESTING

by J.M. Wald

In Fig. 8b, IC_1 is the 8098 micro-controller; crystal X_1 and capacitors C_3 and C_4 are connected to the on-chip oscillator to control the frequency of operation. The unused I/O lines of the 8098 are connected to CN_2 with resistor array RM_1 providing a valid logic low to unconnected inputs. The data bus is 8 bits wide and is time-multiplexed with the lower eight address bits. The octal three-state latch, IC_6, uses the signal ADV to store the lower eight bits of the address at the start of every memory cycle. Circuit IC_7 is an octal, three-state, bidirectional buffer that is used to buffer the data bus. The buffer is enabled for writes at all times except during read cycles: the RD line is used to control the direction.

Circuit IC_8 is a dual 2-to-4 line decoder that provides three memory chip-select signals and four I/O chip-select signals. The ADV signal is used as a strobe to ensure that the chip-select signals are asserted only during valid memory or I/O cycles.

The I/O enable signal on pin 1 of IC_8 is connected to the READY input of the 8098 to force wait states into all I/O cycles. The I/O cycles are limited to two wait states by the value programmed into the CCB. The three unused I/O select lines, CS5, CS6 and CS7 are connected to connector CN_1.

Circuit IC_2 is the monitor EPROM that is enabled for all addresses below 4000 hex.

Circuit IC_4 is a static RAM that is enabled from 8000 hex to BFFF hex.

Circuit IC_3 is either a static RAM or an EPROM that is enabled from C000 hex to FFFF hex.

Both IC_3 and IC_4 are accessed as two 16 K banks and use two PIO output bits to perform the bank selection function.

Circuit IC_5 is a PIO device that provides 16 I/O lines and a number of system control functions. Resistor arrays RM_2 and

8098 Evaluation Board – Component List

Resistors (0.25W, 5%)

R1, 14	2k2
R2, 3	5k1
R4	10k
R5, 6, 7	470R
R8, 11	33k
R9, 12	100k
R10	10M
R13	47k
RM1, 2, 3	47k SIL resistor array

Capacitors

C1, 8, 9, 23	100µ 16V radial electrolytic
C2, 5, 6, 7, 11, 12, 16, 17, 18, 19, 20, 24, 28	100n 16V ceramic disc
C3, 4	33p 16V ceramic disc
C13, 14, 15	390p 16V ceramic disc
C10, 21, 22, 27	470p 16V ceramic disc
C25	22µ 16V radial electrolytic
C26	4n7 16V ceramic disc

Connectors

CN1	BS9525 male IDC 40-way strt skt
CN2	BS9525 male IDC 16-way strt skt
CN3	BS9525 male IDC 20-way strt skt
CN4, 5	7-pin PCB DIN socket
CN6	5-pin PCB DIN socket
CN7	4-way power connector

Semiconductors

IC1	Intel P8098
IC2	2764-2 or 27128-2
IC3	62256-15 or 27128-2 or 27256-2
IC4	62256-15
IC5	P82C55A-2
IC6	74HCT373
IC7	74HCT245
IC8	74HCT139 or 74LS139
IC9	MC1488
IC10	MC1489
IC11	74HC04
D1	1N4148
D2, 3	0A91
ZD1	5V1 Zener
ZD2	6V2 1.3W Zener

Miscellaneous

SW1	SPST push to make PCB switch
X1	7.3728MHz crystal
BZ1	Piezo buzzer
F1	Fuse clip x 2

PCB, IC sockets, through-pins,
+5V, +9V, -9V power supply,
1A quick-blow fuse

890138

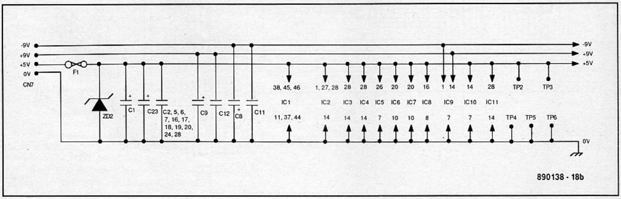


Fig. 8a. Power connexions.

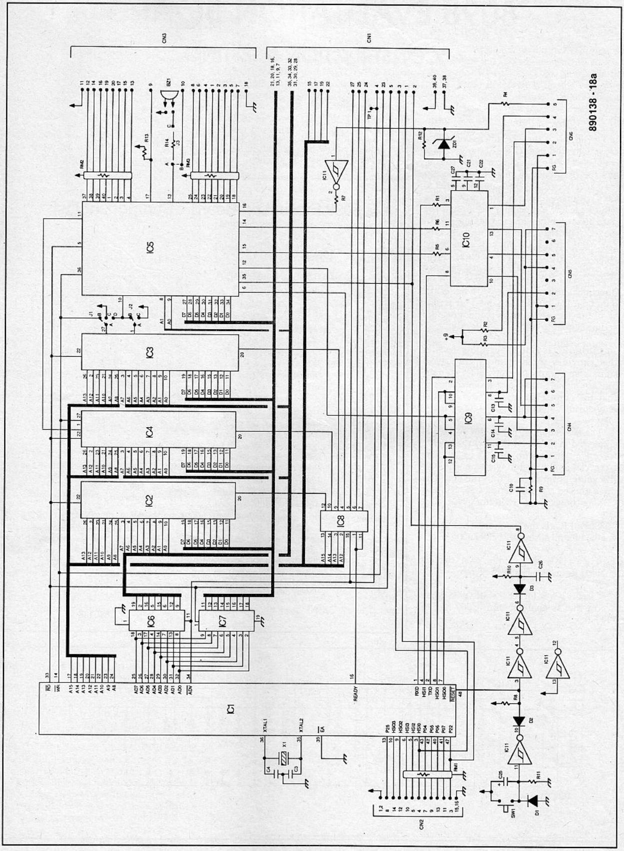


Fig. 8b. The main circuit diagram.

RM$_3$, and resistor R$_{13}$, provide valid logic levels for unconnected PIO lines.

On port 2 of the PIO:

Bits 6 and 7 control the bank selection for IC$_3$ and IC$_4$.

Bit 5 provides an RTS line for the RS232 interface on CN$_4$.

Bit 4 is connected either to the buzzer or directly to CN$_3$. The optional resistor R$_{14}$ limits the current drawn by the buzzer.

Bits 0, 1 and 2 are used as CTS inputs from the three RS232 interfaces on CN$_4$, CN$_5$ and CN$_6$.

Bit 3 is an unused input connected to CN$_3$.

Circuit IC$_{11}$ is a hex Schmitt inverter that generates the reset signal and also converts the RS232 levels on pin 5 of CN$_6$ to the levels required by IC$_5$. Resistor R$_{12}$ and zener ZD$_1$ clamp the input to a maximum of 5.1 V. Negative input voltages are clamped to –0.7 V. Resistor R$_4$ limits the input current to a reasonable value.

The reset signal is generated on power up, when the switch is pressed, or when the 8098 RESET pin is forced low by the occurrence of an internal reset event. Resistor R$_{11}$ and capacitor C$_{25}$ provide the power-up reset delay. Resistor R$_{10}$ and capacitor C$_{26}$ form a monostable to lengthen the short reset pulse produced by the 8098.

Circuits IC$_9$ and IC$_{10}$ are RS232 level shifters. Capacitors C$_{13}$, C$_{14}$ and C$_{15}$ serve to slow down the rise and fall times of the RS232 drivers. Capacitors C$_{21}$, C$_{22}$ and C$_{27}$ provide noise protection on the RS232 receivers. Resistors R$_1$, R$_5$, R$_6$ and R$_7$ provide current limiting if a software fault causes 8098 or PIO pins to switch from input to output mode.

Description of the monitor

The monitor program (see Fig. 7 in last month's article for the hex dump) allows code to be developed on a host computer and then downloaded to the evaluation board and executed. The monitor uses two of the RS232 ports on the board.

Connector CN$_4$ is connected to the host computer aand is used to send commands and data to the board.

Connector CN$_5$ is connected to a printer and can be used to obtain hex dumps.

Connector CN$_6$ is free for use by the application program.

The pin-outs of the RS232 and edge connectors are given in Fig. 9.

Whereas the interface on CN$_6$ uses the 8098 on-chip serial port, the serial ports used for CN$_4$ and CN$_5$ are implemented entirely in software.

The memory map for the evaluation board is shown in Fig. 10. The monitor uses the area from hex 8000 to 85FF in bank 0 of IC$_4$ as working storage. By default, the user stack is located at hex 8800 in bank 0. However, this may be changed with the 'S' command (see below)

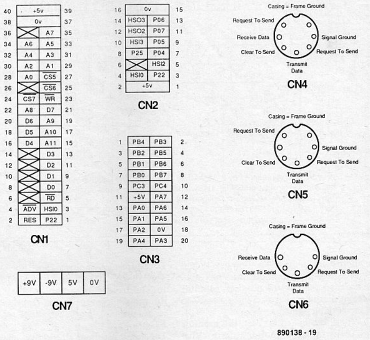


Fig. 9. Connector pinouts (viewed from outside).

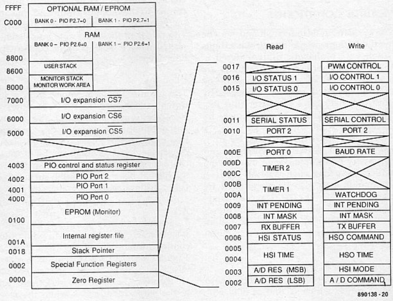
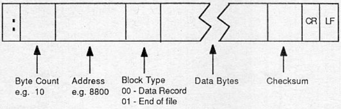


Fig. 10. Memory map of 8098 evaluation board.

Component Overlay (Component Side)

Figure 11 – Intel Hex Record Format



Notes:

- All bytes are represented by 2 ASCII hex characters, most significant nibble first
- The address is represented by 4 ASCII hex characters, most significant byte first
- The Checksum is the two's complement of the sum of all the bytes in the record from the Byte Count to the last data byte
- The Byte Count is the number of data bytes in the record

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to alter the contents of location hex 18 and 19 (SP). Zero-page locations from hex 30 to 5F are also used by the monitor. Monitor sub-routines use the region from hex 1C to 2F as working registers.

When the board is reset, the monitor initializes the system and waits for five seconds for a Carriage Return character (hex 0D) to be sent on CN_4. If a character is received, the baud rate is set to the baud rate of the received character; otherwise, the baud rate defaults to 1200. Baud rates of 110, 150, 300, 600 or 1200 may be used. The printer port (CN_5) defaults to 4800 baud, but this may be changed with the B command.

Monitor commands

Numbers are in hexadecimal and may be entered with the use of hexadecimal digits 1 to 4, with alphabetic digits entered in upper case. If more than four digits are entered, only the last four are used. The last digit entered may be cancelled by sending a Backspace character (hex 08). The monitor responds to a backspace by echoing "\".

Numbers must be separated by commas or spaces. A partially entered command may be abandoned by entering an illegal character, such as a plus sign (+). Commands may also be abandoned by entering CTRL>C (hex 03). The commands are described below, where <CR> represents a Carriage Return character and an item enclosed in angle brackets <...> represents a number.

B <baud rate> <CR>
The printer port (CN_5) baud rate is set to <baud rate>, which is one of 300, 600, 1200, 2400 or 4800.

C <bank> <CR>
This command is used to change the bank accessed from IC_3, the optional RAM or EPROM. <bank> must be 0 or 1

D <address1>, <address2> <CR>
The contents of locations from <address1> to <address2> are displayed as a hex dump with 8 bytes per line.

E
The monitor echoes all received characters until a <CTRL>C character is received.

G <address1>, <address2> <CR>
This command starts execution of the user program from <address1>. If <address1> is omitted, the last break point address is used. If <address2> is supplied, a break point is set at <address2>. Providing that the HSI and Software Timer interrupts are enabled, entering <ESCAPE>(hex 1B) returns control to the monitor command line and the values of PC, SP and PSW are displayed. The values of these registers are also displayed when a break point or TRAP instruction is reached.

L
The monitor loads memory from a file downloaded from the host computer in Intel Hex format (see Fig. 11). The monitor will automatically return to the command line if an End-of-File record is received; otherwise, the user must send a <CTRL>C character to terminate the command. After the file has been received, the current execution address of the program is displayed

R
This command may be used to generate a system reset. The monitor will prompt for confirmation by displaying "Reset? (Y/N). Type 'Y' to perform a system reset, otherwise type 'N'. Any other characters entered are ignored. The command performs exactly the same function as when the reset switch is pressed and may be used to return the system to a known state.

S <address> <CR>
The monitor displays the contents of the location at <address>. The next location may be displayed by entering "/". The previous location is displayed by entering "-". The current location can also be changed by entering "=" or "@" followed by the new address and then <CR>. The contents of the current location can be changed by entering the new data followed by <CR>. The newly entered data is verified and, if the location fails to verify, the monitor will display "?".

T <address1>, <address2> <CR>
This is the same as the D command except that the hex dump is sent to the printer port (CN_5) and has 16 bytes per line.

V
This is the same as the L command except that the downloaded file is verified against the contents of the memory instead of replacing the contents of the memory. The command will display the address of any locations that do not verify.

Construction

The evaluation board is constructed on a double-sided printed-circuit board (see Fig. 12).

The first step is to insert all the through pins and ensure that they are soldered on both sides of the board. It is important to double-check this carefully, since it will be virtually impossible to rectify any errors once the other components are in place.

The next step is to solder in the two insulated wire links, LK_1 and LK_2, followed by the diodes and all the resistors, except R_{14}. Check that the diodes are inserted the correct way round. Solder the capacitors, fuse clips and crystal in place; make sure that the electrolytic capacitors are inserted the right way round.

Note that some components must be soldered to pads on both the top and underside of the board.

Finally, solder the IC sockets, connectors and reset switch in place.

The board allows for a number of options.

Firstly, IC_3 may be be a Type 62256 static RAM or Type 2764, 27128 or 27256 EPROM. Depending on the type of chip used, jumpers J_1 and J_2 must be set as shown in Fig. 13.

Secondly, a piezo-electric buzzer may be fitted. Fit resistor R_{14} and solder the buzzer leads to the points indicated in Fig. 14. If a buzzer is not wanted, fit link LK_3 instead.

Checking & testing

Check the board for short-circuits, especially between the power supply lines. Check also for continuity between IC socket pins, using the circuit diagram in Fig. 8a to identify the pins that are connected to each other. Ensure that there are no misplaced components or components inserted the wrong way round.

Insert the fuse and connect the power suply to connector CN7 (see Fig. 9). The

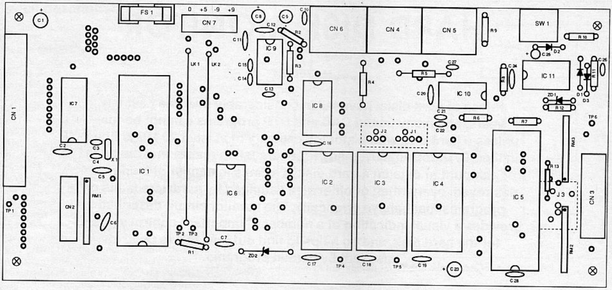

Fig. 12. Printed circuit (component overlay) for the 8098 evaluation board.

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power supply must provide +5 V ±5% at 500 mA; +9 V ±10% at 100 mA; and -9 V ±10% at 100 mA. Turn the supply on and check that the correct voltages appear on the power supply pins of the IC sockets.

If all is well, turn the supply off, wait for the power supply capacitors to discharge, and then insert IC_{11}. Turn the supply on again and check that pressing the reset switch generates a negative pulse on pin 48 of IC_1 and a positive pulse on pin 35 of IC_5. Turn the supply off again, wait for the capacitors to discharge, and then insert IC_1 and ICs_{3-10}.

Insert a Type 2764 or 27128 EPROM containing the code listed in Fig. 7 in the position marked for IC_2. If you use a Type 2764, you should subtract hex 2000 from the addresses listed down the side of the hex dump.

Finally, turn the supply on and check that the board sends the following message down the RS232 interface on CN_4 at 1200 baud:

```
8098 Monitor V1.8 by J.M. Wald 1989

>
```

Further reading

The following Intel Data Books are a useful source of information on the 8098, and the 8096 family in general.

8-bit Embedded Controller Handbook, Intel 270645, 1989.

16-bit Embedded Controller Handbook, Intel 270646, 1989.

Embedded Controller Applications Handbook, Intel 270648, 1989.

The section entitled "Using the 8096" in the *16-bit Embedded Controller Handbook* contains a number of useful examples of 8096 code, including examples of a Software Serial Port and a Multiple Channel Pulse Width Modulator.

The address of Intel in the United Kingdom is: **Intel Corporation (UK) Ltd, Pipers Way, SWINDON SN3 1RJ, Telephone (0793) 696000.**

Acknowledgments

INTEL is a trademark of Intel Corporation, USA. HMOS and CHMOS are patented processes of Intel Corporation, USA.

EPROM & source coding

Readers are advised that a programmed EPROM and the source coding for the 8098 evaluation board are available from Mr J.M. Wald via the London Offices of Elektor Electronics (Publishing). Note that all payments for these should be addressed to Mr J.M. Wald. Films of the PCB to Mr Wald's design are available from our London offices.

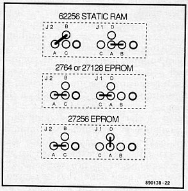


Fig. 13. IC3 jumper settings

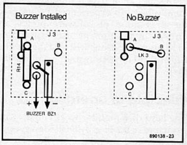


Fig. 14. Optional buzzer.

HARD DISK MONITOR

M. Noteris

Prices of hard disks have fallen considerably over the past few years, and many useful CAD and DTP programs can not be run unless a hard disk with a storage capacity of at least 20 MB is fitted in the PC. Unfortunately, many PC users fail to realize that the huge amount of data on a hard disk is always in danger of being destroyed, overwritten or otherwise damaged by hardware faults or programs that behave erratically. The monitor circuit described provides a visual indication of a number of important control signals for the hard disk, and so helps to find out how this is used (or misused) by certain programs.

PC users have good reason to start worrying when the hard disk falls silent after a series of rapid access operations by a program or installation procedure from the keyboard. In the worst case, the screen goes blank, and the machine no longer responds to keyboard commands. Die-hard PC users describe this condition as BRST (big red switch time), and can only keep smiling, hoping that the computer will boot up again. Since this involves loading the auto-execute and system configuration files from hard disk, a dead silent computer after a 'cold boot' is a real cause to start worrying, digging up the installation manual and, most importantly, looking for the back-up floppy disks.

Hard disk malfunctions, boot-up problems and loss of files, programs and whole directories need not always be caused by hardware faults. While it can not always help to prevent disaster, the monitor circuit described here helps to keep an eye on the hard disk activities of certain programs. As such it is a diagnosis instrument offered to experienced PC users for the prevention of software piracy and viruses. In addition, PC users specialized in hardware add-ons will find the monitor a useful aid for testing and installing hard disks.

Principle of operation

The hard disk monitor works on the same principle as the Floppy Disk Monitor published a few months ago (Ref. 1). The block diagram of Fig. 1 shows that the monitor circuit is composed of buffers, counters, decoders and a display section. The number of LED displays is, of course, greater than with the Floppy Disk Monitor. The hard disk monitor is connected in parallel to the cable that carries the control signals between the controller card and the hard disk drive in the PC. The pinning and signal designations on the Shugart control bus (ST506) for hard disk drives is given in Fig. 2.

HARD DISK MONITOR

- Real-time indication of current cylinder on 4-digit LED read-out
- Supports up to 1,024 cylinders
- Head number indication with LEDs
- Adjustable response time of cylinder read-out
- For all ST506 compatible hard disk drives
- 'Seek Complete; indication
- 'Disk Ready' indication
- 'Write Enable' indication
- 'Fault' indication
- Compact unit to fit in 3½-inch drive slot
- Powered by computer

The count range of the monitor is 1,024, or equal to the maximum number of cylinders (tracks) that can be selected by a standard PC-AT computer (note, however, that certain controllers are capable of addressing up to 1224 cylinders). The counter block in Fig. 1 is, therefore, composed of four decimal counter circuits cascaded via their CARRY OUT and CARRY IN lines.

Since every modern hard disk drive has more than two heads, it is interesting to know the side and the number of the internal disk being written to or read from. The ST506 hard disk control bus has four lines for the selection of a maximum of 16 heads. To visualize the current head number, the four-bit binary head selection code is applied to a decoder with LEDs connected to its outputs.

Most hard disk controller cards allow the use of two drives, which can be addressed individually by a selection code on the command bus. The hard disk monitor has a jumper, J3, to select the desired drive.

Signals and timing

The diagram of Fig. 3 shows the timing of the main signals on an actuated hard disk bus of a PC-AT computer. The timing of the signals shown forms the basis for the design of the hard disk monitor, and will be examined below

A difficulty may arise when DIRECTION changes state on the positive edge of the STEP signal. Since the DIRECTION signal is connected to the U/$\overline{D}$ (up/down) input of the track counter, this must be clocked by the trailing edge of the STEP signal.

The TRACK0 signal is used to synchronize the 4-digit track counter to the actual position of the heads. The first STEP pulses may occur at the same time as the actuated TRACK0 signal. This means that TRACK0 may not be used to control the RST (reset) inputs of the counters direct. A monostable is, therefore, used to shorten the TRACK0 pulses to about 0.5 ms, so that the counters are clocked reliably by the STEP signal.

Circuit description

The circuit diagram in Fig. 4 shows that the ST506 bus signals are applied to the monitor circuit via connector K$_1$. Three-state inverting bus drivers IC$_1$ and IC$_2$ are controlled by the DRIVE SELECT signal brought to their G1-G2 (enable) inputs via jumper J$_3$. The TRACK0 signal is inverted and applied to monostable IC$_{3A}$, which in turn resets the counters.

When the hard disk drive is not selected, the outputs of the bus drivers are switched to the high-impedance mode. Resistor R$_{16}$ at the input of Schmitt trigger NAND gate IC$_{13C}$ then ensures that the clock inputs of the counters are held logic high. When the hard disk selected with J$_3$ is accessed by the computer, IC$_1$ and IC$_2$ invert the signals on connector K$_1$. The STEP signal is first logic high (= not actuated), so that the counter clock signal does not change state. After a short delay introduced by monostable IC$_{3A}$, the STEP signal is applied to the counter clock inputs, with its original polarization (both IC$_2$ and IC$_{3A}$ are inverters). The cascaded counters are advanced by the trailing (positive) edge of the STEP pulses.

Counters

The output signal of gate IC$_{13C}$ is applied to the clock inputs of counters IC$_5$ through IC$_8$, and to one input of gate IC$_{13D}$, of which the function is discussed further on.

The DIRECTION signal is taken direct to the U/$\overline{D}$ inputs of the four counters. These are Types 4510 with a built-in BCD encoder.

BCD-to-7 segment decoder

The outputs of the counters are connected direct to the corresponding inputs of BCD-to-7 segment decoders/display drivers IC$_9$ through IC$_{12}$. The outputs of these chips Type 4543 need only a series resistor to sink the typical segment current of a LED display segment. High-intensity common-anode LED displays Type HD1131O from Siemens are used for a clear 4-digit track number indication.

Decimal points

The decimal points on the four 7-segment displays are used to indicate actuation of certain control signals for the hard disk drive.

The WRITE FAULT signal is actuated briefly when a wrong byte is written to the hard disk. The signal is lengthened to about 1.5 s by a monostable composed of NAND gates IC$_{13A}$ and IC$_{13B}$. Their output signal controls the decimal point on display LD$_3$.

The functions of the three remaining indicators, WRITE, SEEK and READY, require no further discussion.

Head selection

The selected head in the hard disk drive is indicated by LEDs D$_1$ through D$_{16}$. In most cases, the actual number of LEDs used will be four or five, depending on the number of heads in the hard disk drive (in case of doubt, consult the documentation). In general, only hard disk drives with a storage capacity of 100 MByte or more have 10 or more heads. The head select code is taken from the HEAD SELECT 2^0, through HEAD SELECT 2^3 lines of the ST506 bus, and is converted to an active-low one-of-16 signal by decoder IC$_4$.

In case lines HEAD SELECT 2^2 and HEAD SELECT 2^3 are not used, they may be made logic high at the inputs of IC$_1$ by fitting wire jumpers JP$_1$ and JP$_2$. Also note that some manufacturers of disk controller cards use the ST506 bus lines connected to pins 2 and 4 of K$_1$ for purposes other than head selection.

The terminal marked L in the circuit diagram forms the central supply point for the LED displays.

Mode selection

The FAST/SLOW mode selection switch

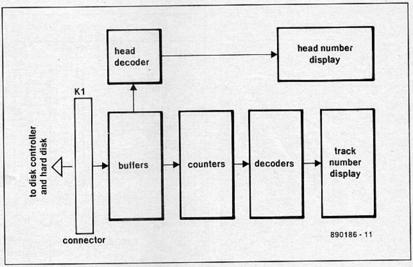
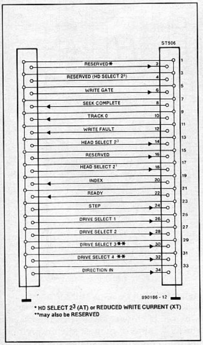


Fig. 1. Block diagram of the monitor for ST-506 compatible hard disk drives.



* HD SELECT 2^3 (AT) or REDUCED WRITE CURRENT (XT)
**may also be RESERVED

Fig. 2. ST-506 bus signal assignment.

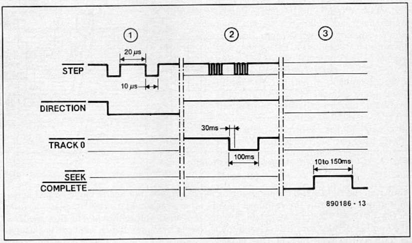


Fig. 3. Timing of the main signals in the hard disk monitor circuit.

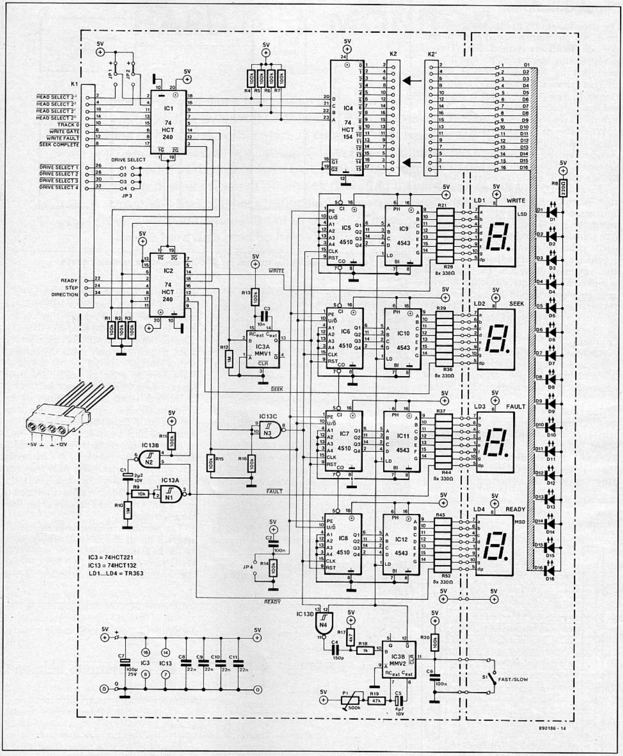


Fig. 4. Circuit diagram of the hard disk monitor.

shown in the right-hand corner of the circuit diagram controls the response speed of the displays. When the switch is closed, the number of the currently accessed track is indicated in real time. During normal use of the hard disk — that is, after the low-level and high-level formatting procedures — the heads move so fast across the tracks that the display reading becomes unintelligible. The slow mode selected by opening S₁ enables the user to reduce the rate of change of the track read-out by setting potentiometer P1. Capacitor C₅ may be increased if the maximum delay that can be set is still too short.

The FAST read-out mode is enabled when S₁ is closed. The switch then takes the $\overline{\text{CLR}}$ input of monostable multivibrator MMV₂ to ground, so that the LD (latch disable) inputs of the display drivers are actuated. This results in the display dri-

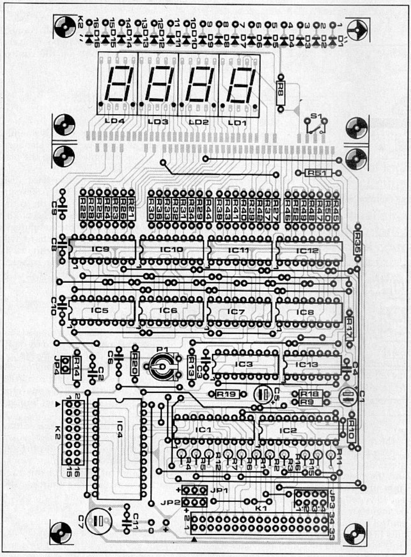


Fig. 5. Component mounting plan of the printed-circuit board. The display and control sections are separated by cutting the board along the dashed line at the component side.

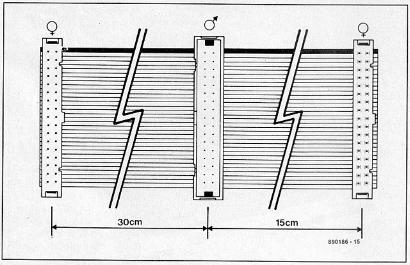


Fig. 6. Home-made cable to connect the hard disk monitor on to the ST-506 bus.

Parts list

Resistors:
$R_1 - R_7$;$R_{11} - R_{16}$;R_{18};R_{20} = 100k
R_8 = 220Ω
R_9 = 10k
R_{10};R_{12} = 1M0
R_{17} = 4k7
R_{19} = 47k
$R_{21} - R_{52}$ = 330Ω
P_1 = 500k preset H

Capacitors:
C_1 = 2μ2; 10 V
C_2;C_6 = 100n
C_3 = 10n
C_4 = 150p
C_5 = 4μ7; 10 V
C_7 = 100μ; 25 V
$C_8 - C_{17}$ = 22n

Semiconductors:
$D_1 - D_{16}$ = red LED (3 mm)
$LD_1 - LD_4$ = HD1131O (Siemens)
IC_1;IC_2 = 74HCT240
IC_3 = 74HCT221
IC_4 = 74HCT154
$IC_5 - IC_8$ = 4510
$IC_9 - IC_{12}$ = 4543
IC_{13} = 74HCT132

Miscellaneous:
K_1 = 34-way straight pin header (double row) and mating IDC cable socket.
S_1 = miniature SPST switch.
PCB Type 890186

vers becoming transparent, i.e., they pass the binary input code immediately to the built-in 7-segment decoders with associated LED drivers.

In the SLOW read-out mode, IC_{3B} forms an oscillator that supplies short pulses to the LD inputs of the display drivers. These pulses cause the applied 4-bit binary code to be latched and displayed until the next LD pulse arrives.

To make sure that only valid track data is stored and displayed, NAND gate IC_{13D} combines the output signal of MMV IC_{3B} with the STEP signal. This arrangement prevents the display latch control signal (the rising edge of the LD pulse) occurring at the instant the counters change state.

Hard disk drive selection

Jumper JP_3 is fitted in position 1 or 2 to select the required hard disk drive. Swap the jumper setting if you do not know which drive selection signal is used by the hard disk controller card in your computer. Also note that the first hard disk in the system is sometimes referred to as 0, the second one as 1, etc.

Hardware reset

IBM PCs and compatibles boot from track 0. The TRACK0 signal is actuated and resets the counters in the hard disk monitor almost immediately after the computer is switched on. Although this reset pulse has a well-defined length, the hard disk monitor has a hardware reset circuit,

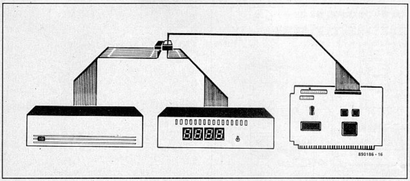


Fig. 7. Showing the connection of the hard disk monitor between the disk controller card and the hard disk drive.

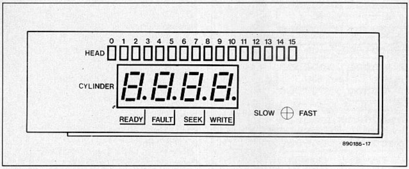


Fig. 8. Suggested front-panel layout.

R_{14}-C_2, which is useful for experimental purposes. Normally, however, this circuit is inoperative because its output pulse length is shorter than that of the TRACK0 pulse after the computer is switched on. The hardware reset circuit may be disabled by fitting jumper JP_4.

Construction

The availability of a ready-made printed circuit board should enable any one with some experience in working with electronics circuits to build a working hard disk monitor.

The size of the printed circuit board (Fig. 5) is geared to that of a 3½-inch floppy disk drive. Most modern PCs allow this type of disk drive to be installed in a number of locations.

Start the construction by cutting the board along the dashed line to separate the display section from the control section. The boards are later mounted at right angles.

Fit all wire links on the control board, using solid insulated wire. Then fit the components on to the board, checking the value, type number and orientation against the parts list and the component mounting plan printed on the board. Sockets are not strictly required for the integrated circuits.

Mount a 40-pin IC socket on the display board to accept the four LED displays. Next, determine how many LEDs you need for the HEAD NUMBER indication, and fit these parts starting at the left side of the displays.

Use two 10×45 mm aluminium angle pieces and the holes in the display board and the control board to mount these at right angles as shown in the photographs. The lower edge of the display board must be about 3 mm below the track side of the control board. Align the boards horizontally to enable pairs of facing copper track ends to be joined by soldering. After soldering, use a magnifying glass to check for short-circuits between adjacent tracks.

Use flexible, light-duty wire to connect the terminals on the display board to the corresponding terminals on the control board.

Power supply and connection

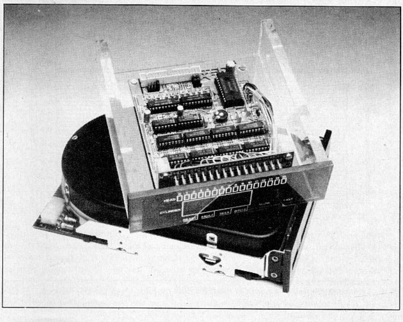
The hard disk monitor is conveniently powered by the computer via a standard disk drive power connector (see the pinning diagram inset in Fig. 6).

The drive signals for the hard disk monitor are obtained from the ST506 control bus. Connectors are fitted on to the flat ribbon cable as shown in Fig. 6. The connection of this cable in the computer is further illustrated in Fig. 7. The hard disk monitor may also be used with hardcards, but only if the connection between the hard disk and the controller card is accessible.

Final points

If a 20 MByte hard disk drive is used, the cost of the circuit may be reduced by omitting IC_8, IC_{12} and LD_4 (with only 616 cylinders, there is little point in using the fourth digit). The READY indication is taken over by a discrete LED, connected to pin 3 of IC_2 via a 220 Ω current limiting resistor.

The hard disk file location and editing functions provided by the well-known Norton Utilities are fine for testing the operation of the hard disk monitor, whose read-out should correspond to the track information shown on the monitor.



INTRODUCTION TO DIGITAL SIGNAL PROCESSING

by Brian P. McArdle

Digital circuits are usually considered to be easier to understand than analogue ones because they consist of logic gates that can be explained with Boolean algebra. All such circuits may be reduced to a combination of AND, OR and INVERTER (NOT) operations. But from the point of signals, the purpose of digital circuits is to process digital signals and consequently the important topic called Digital Signal Processing has become an essential course in the training of engineers and technicians. The purpose of this article is to explain the differences and similarities between the techniques used to analyse analogue and digital signals. It is only a basic introduction and readers who require a detailed study should consult the many textbooks on the subject.

Analogue signal processing

Before considering digital signals, a review of the techniques used to analyse analogue signals will avoid confusion later on. In the following three sub-sections it is assumed that the signals are continuous with respect to time (i.e., are in a time continuum).

1. Consider a voltage signal $v(t)$ where t refers to time. This can be expressed in terms of frequency by using the **Fourier Transform** as follows.

$$V(\omega) = \int_{-\infty}^{\infty} v(t)\,\mathrm{e}^{-j\omega t}\,\mathrm{d}t. \qquad [1]$$

The result is that the angular frequency, ω, has become the variable instead of t. Hence, the effect of the transform is to change a signal from the **time domain** to the **frequency domain**. The **Inverse Fourier Transform** is

$$v(t) = 1/2\pi \int_{-\infty}^{\infty} V(w)\,\mathrm{e}^{j\omega t}\,\mathrm{d}\,\omega. \qquad [2]$$

In the special case where $v(t)$ is periodic, the **Fourier Series** can be used as follows

$$v(t) = \sum_{n=-d}^{\infty} \mathrm{C}_n \mathrm{e}^{j\omega t} \qquad [3]$$

and

$$\mathrm{C}_n = \frac{1}{T}\int_{-T/2}^{T/2} v(t)\,\mathrm{e}^{-j\omega t}\,\mathrm{d}t. \qquad [4]$$

Although the transforms and series can be difficult to apply to complex signals, they are important tools of signal analysis.

2. Consider the circuit in Fig. 1. The input and output signals with respect to time are $v(t)$ and $v_C(t)$ respectively. The most common method of analysis is to use the **Laplace Transform** described by the equation

$$V(s) = \int_0^{\infty} v(t)\,\mathrm{e}^{-st}\,\mathrm{d}t. \qquad [5]$$

The transform changes the signal from the t-domain to the s-domain and the variable s is complex. From the point of analysis, the capacitor may be considered as a component of impedance $1/sC$ as illustrated in Fig. 2. Note that if the capacitor were replaced by an inductor L, the impedance would be sL instead of $1/sC$. The voltage and current expressions are transformed as per equation [5] and the circuit is now a simple voltage divider with

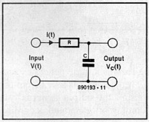


Fig.1. Low-pass filter

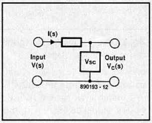


Fig. 2. Voltage divider

$$V_c(s) = \left[\frac{1/sC}{R + 1/sC}\right] V(s) = \frac{V(s)}{1 + sRC}. \qquad [6]$$

In the particular case where the input is sinusoidal, the frequency response can be deduced by substituting $j\omega = s$ in equation [6]. This is but a simple example, but it nevertheless demonstrates the importance of the Laplace Transform.

3. The **Autocorrelation Function** of a signal $v(t)$ is given by

$$R(\tau) = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} v(t)\,v(t \pm \tau)\,\mathrm{d}t. \qquad [7]$$

Its importance is best illustrated by considering an example, $v(t) = A\cos(\omega t)$ which, when substituted in equation [7], gives

$$R(\tau) = \frac{\mathrm{A}^2}{2}\cos(\omega\tau). \qquad [8]$$

The maximum value occurs at $\tau = 0, T, 2T, 3T$, and so on. In other words, if $v(t)$ is periodic, $R(t)$ is also periodic with the same period. The main applications are the checking of signals for periodicity and the detection of signals corrupyed by noise. If instead of $v(t)$ equation [7] has two different signals $v_1(t)$ and $v_2(t \pm \tau)$, $R(\tau)$ is know as the **Crosscorrelation Function.**

Digital signal processing

Digital signals can either be in digital form from the beginning (i.e., from the source) or analogue signals that undergo an analogue-to-digital conversion. The next two sub-sections consider the analysis of digital signals from these two viewpoints and illustrate the changes required in the various formulas for analogue signals discussed above.

1. Consider the arrangement in Fig. 3. This is a linear feedback shift register of four stages. Each stage is a JK bistable (flip-flop) with a truth table as shown in Fig. 4. The shift register is provided with a seed (e.g., 0101) and the feedback logic generates successive states from this initial state. If the output is taken from the 4th bistable as shown in the diagram, the output is actually a binary sequence $\{a_n\}$ with the incoming bit generated according to

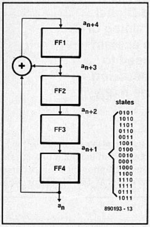
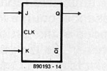


Fig. 3. Linear feedback shift register with four stages.



a_{n-1}	J	K	a_n
0	0	0	0
	0	1	0
	1	0	1
	1	1	1
1	0	0	1
	0	1	0
	1	0	1
	1	1	0

Fig. 4. JK bistable (flip-flop).

$$a_{n+4} = (a_n + a_{n+3}) \bmod 2 \qquad [9]$$

for $n \geq 4$. In electronics terms, modulo 2 is an exclusive or logic operation. The sequence of states repeats after 15 steps, which means that the output sequence $\{a_n\}$ has period 15. To be precise, this is a maximum length sequence ($2^4 - 1 = 15$), because the state (0, 0, 0, 0) is not used for linear feedback shift registers. The period is determined by the feedback logic, but this particular point need not be considered. At this stage, the Fourier Transform and Laplace Transform have no relevance, but the Autocorrelation Function is of special interest. The binary sequence $\{a_n\}$ is periodic and its Autocorrelation Function should therefore peak at a shift of 15.

Obviously, equation [7] is not suitable and the following amended version is used (in which k is used rather than τ to indicate the extent of the shift).

$$R(k) = \frac{1}{N} \sum_{i=1}^{N} a_i a_{i+k}. \qquad [10]$$

For the output sequence {1, 0, 1, 0, 1, 1, 0, 0, 1, 0, 0, 0, 1, 1, 1}, the values are:

k:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
$NR(k)$:	8	4	4	4	4	4	4	4	4	4	4	4	4	4	4	8	4	4	4	4	4	4	4

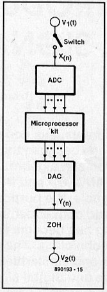


Fig. 5. Digital signal processing network.

The peak values occur at $k = 0$ and 15 as expected. An interesting point is that $R(k)$ is two-valued. This is a property of maximum length linear feedback shift registers, because they generate approximately equal numbers of 1s and 0s. In the example there are eight 1s and seven 0s.

It should be noted that the analysis does not make any reference to voltages, currents or impedances, which would be expected in the analysis of analogue signals or circuits. Once the circuit operates as a digital circuit, only the logic levels need to be considered.

2. Consider the arrangement in Fig. 5. This has both analogue and digital signals at various stages. The output $v_2(t)$ is not derived directly from input $v_1(t)$. The input is sampled to produce a discrete time signal. The switch represents a sampling operation that in turn can be represented mathematically by a delta function:

$$x(n) = v_1(t)\delta(t - nT). \qquad [11]$$

This means that the samples are taken every T seconds with $n = 1$ as the first sample and so on. There is a specific condition that samples must be taken at a rate at least twice the maximum frequency of $v_1(t)$ to avoid aliasing. However, before it can be processed as a digital signal, it must be turned into a binary number by the analogue-to-digital conversion operation. In mathematical terms, this can be written:

$$x(n) = \left[X_0, X_1, X_2, \ldots, X_{N-1}\right] = \sum_{i=1}^{N-1} X_i 2^i. \qquad [12]$$

Thus, N bits are required to represent each discrete signal with X_0 and X_{N-1} as the LSB and MSB respectively. Two points are of importance:

(a) if, at any time during the sampling operation, $x(n)$ has a value in excess of (2^{N-1}), additional bits are required;

(b) if negative values have to be distinguished from positive values, the negative values are represented by the 2's complement of the positive representations. This would mean that (N+1) bits are required for the full range of values. The extra bit could be considered as a sign bit (e.g., "0" and "1" for positive and negative values respectively).

In the example, the output from the A-to-D converter is input into a microprocessor kit, but any item of digital signal processing equipment would suffice. The output after the D-to-A converted $y(n)$ corresponds to the processed $x(n)$. The delay between inputting $x(n)$ and obtaining $y(n)$ is the processing time required for each discrete signal. In real time, the system could not operate faster than this processing time.

What relevance do the transformations introduced under 'Analogue signal processing' now have?

(i) The Fourier Transform would have to be amended from the version in equation [1] as follows:

$$X(n) = \frac{1}{N} \sum_{m=0}^{N-1} x(m) e^{-j2\pi mn/N} \qquad [13]$$

in which n goes from 0 to $(N-1)$. The factor $1/N$ is for normalization. A further development of this expression is the basis for the Fast Fourier Transform (FFT) which is not considered in this article.

(ii) Instead of the Laplace Transform, the **Z Transform** is used. Consider equation [12] again. The Z Transform is given by the equation

$$X(z) = \sum_{n=-\infty}^{\infty} x(n) z^{-n} \qquad [14]$$

in which very often only values of $n \geq 0$ are considered. For the remainder of this article it is assumed that this restriction applies. The transform has turned the sequence $\{x_n\}$ into a series. Its main application is in **digital filters** discussed later in this article. The relationship between z and the Laplace variable s is $z = e^{sT}$. The transform is particularly important for the entire area of Digital Signal Processing.

An important point about the z transform is the shift property. Suppose $y(n) = x(n-1)$, where each term is delayed by one step.

$$\therefore Y(z) = \sum_{n=1}^{\infty} y(n) z^{-n} = y(1) z^{-1} + y(2) z^{-2} + \ldots + y(n) z^{-n} \qquad [15]$$

There is no $y = 0$ since $x(0) = y(1)$ is the first term. Substituting for the $y(n)$'s gives

$$Y(z) = x(0) z^{-1} + x(1) z^{-2} + \ldots + x(n-1) z^{-n} = z^{-1} X(z) \qquad [16]$$

Therefore, z^{-1} represents a delay of one step. (This is similar to analogue circuits where a delay of T seconds is given by e^{sT}, but in practice a first order lag $1/(1+sT)$ is used as an approximation). In the same manner, $y(n) = x(n-m)$ results in $Y(z) = z^{-m} X(z)$ corresponding to a shift of m steps.

Digital filters

Digital filters deserve special mention. Firstly, the word 'filter' may be misleading. Analogue filters operate in the **frequency domain**. They filter out or remove certain frequencies (like the low-pass filter in Fig. 1) that are not required or wanted at the output. Digital filters are quite different. There are two main categories as explained by the following examples.

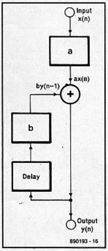


Fig. 6. Recursive filter

(1) The circuit in Fig. 6 is a **recursive filter** whose output $y(n)$ depends not only on $x(n)$, but also on the previous output $y(n-1)$. The operation may be described by the equation

$$y(n) = ax(n) + by(n-1) \qquad [17]$$

The use of the Z Transform and the shift property gives

$$Y(z) = aX(z) + bz^{-1} Y(z) \qquad [18]$$

$$= \frac{a}{(1 - bz^{-1})} X(z) \qquad [19]$$

In electronic terms, the binary representation of $x(n)$ and $y(n-1)$ would be processed by a microcomputer (section b under 'Digital signal processing'). This particular example uses the output of the immediate previous stage, but any previous stage or combination of stages could also be used. The only requirement is that the output at any stage must depend on previous outputs. If $X(z)$ is known, $Y(z)$ can be calculated, followed by $y(n)$ from the **Inverse Z Transform**. For example, suppose $x(n) = 1$ for $n \geq 0$, which is the equivalent of a unit step at $t = 0$ in analogue circuits:

$$X(z) = \frac{1}{(1 - z^{-1})}. \qquad [20]$$

From **partial fraction decomposition**:

$$Y(z) = \frac{A}{(1 - bz^{-1})} + \frac{B}{(1 - z^{-1})} \qquad [21]$$

With $A = ab/(b-1)$ [22]

and $B = a/(1-b)$, [23]

$\therefore$ $y(n) = Ab^n + B$. [24]

(2) The circuit in Fig. 7 is a **non-recursive filter**. The output depends on the input and the previous input according to

$$y(n) = ax(n) + bx(n); \qquad [25]$$

$$Y(z) = (a+bz^{-1})X(z). \qquad [26]$$

For $x(n) = 1$ and $n \geq 0$, equation [26] can be rewritten as

$$Y(z) = \frac{a + bz^{-1}}{1 - z^{-1}} = \frac{a}{1 - z^{-1}} + z^{-1} \cdot \frac{b}{1 - z^{-1}} \qquad [26a]$$

Since z^{-1} is a delay,

$$y(0) = a \qquad [27]$$

and

$$y(n) = a + b \qquad \text{for } n \geq 1. \qquad [28]$$

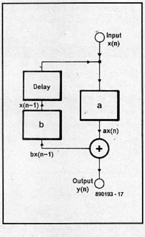


Fig. 7. Non-recursive filter

This result agrees with an intuitive understanding of the circuit; the output is stepped up at first by a and finally by (a+b).

Both examples are intended to explain the various operations and do not represent specific processes. Note the difference between equations [19] and [26]. The apparently simple change of feeding back the unprocessed signal, i.e., $x(n-1)$ instead of $y(n-1)$ produces a totally different type of filter with a major difference in behaviour and response.

Note that the terms **finite impulse response** (FIR) and **infinite impulse response** (IIR) may be used instead of non-recursive and recursive respectively.

Kalman filter

The arrangement in Fig. 8 is known as a **Kalman filter**. It operates as a **recursive estimator**. While 'recursive' requires no explanation, it is clear that 'estimator' implies that values have been approximated and may not be accurate. The term $\hat{y}(n)$ at the

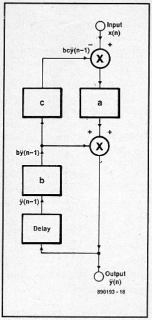


Fig. 8. Kalman Recursive Estimator

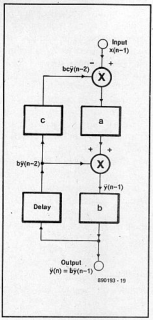


Fig. 9. Kalman Recursive Predictor

output represents a value close to, but not equal to, $y(n)$. In mathematical terms:

$$\ddot{y}(n) = y(n) + \varepsilon(n), \qquad [29]$$

where $\varepsilon(n)$ represents the error that could be caused by additive noise, and so on. If $x(n)$ is the input at stage n, representing an observed or measured value, the output is given by:

$$\ddot{y}(n) = \mathrm{a}[x(n) - \mathrm{bc}\ddot{y}(n-1)] + \mathrm{b}\ddot{y}(n-1). \qquad [30]$$

The first part of the right-hand side of equation [30] represents a correction factor to the overall recursive operation. In other words, the process is designed to have $\ddot{y}(n)$ approximated by $\mathrm{b}\ddot{y}(n-1)$ plus a correction. Parameters a, b and c are chosen to minimize the **mean square error**. Usually, b and c are constants, whereas a varies with n and is written as $a(n)$ in most textbooks.

Figure 9 shows a **recursive predictor**, which, instead of deducing $\ddot{y}(n)$ from $\ddot{y}(n-1)$ and $x(n)$, attempts to predict $\ddot{y}(n)$ from $\ddot{y}(n-1)$ and $x(n-1)$. This is a one-step predictor, i.e., it predicts just one step ahead of the input. Parameters a, b and c are chosen to minimize the MSE as in the previous case. Since the input would normally be random, the correction term would be small enough to allow the predicted $\ddot{y}(n)$ to be taken as $\mathrm{b}\ddot{y}(n-1)$. The main application of this circuit is in **tracking**, and so on. Readers who require a detailed analysis of these networks should consult Ref.(2).

Conclusions

The entire area of Digital Signal Processing has blossomed during the past ten years. Future developments are too difficult to predict, but the fundamental ideas outlined in this article should be known by every engineer and technician. The trick is to have a clear hold on the ideas so that they are understood like basic transistor circuits. If it appears that an engineer or technician involved solely in digital electronics does not need to know Ohm's law, that is an exaggeration. Fundamental ideas still apply in analogue and digital circuits alike.

References

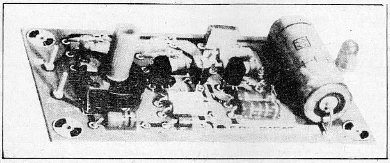
Signal Processing: Discrete Spectral Analysis, Detection and Estimation by Mischar Schwartz and Leonard Shaw; McGraw Hill (USA) 1975.

Digital and Kalman Filtering by S.M. Bozic; Edward Arnold, London, 1979.

Signal Processing: Principles and Applications by D. Brook and R.J. Wynne; Edward Arnold, London, 1988.

Editor's note: Readers may also find *Circuits, Signals and Devices* by Michael Julian (Longman Scientific and Technical - 1988) of interest.

Loudspeaker peak indicator



Nowadays, any decent loudspeaker unit is, fortunately, pretty resistant to rough treatment. However, problems can arise in the living room when the volume is turned up high enough for clipping to occur. At that point substantial distortion and higher harmonics can be generated. This does not only spoil listening pleasure but it can actually damage the tweeters. A measure of protection can be acheived by the use of a clip or peak indicator, an extra not yet normally included in the majority of audio amplifiers.

The peak indicator described here can be connected directly to the output of the amplifier or even fitted into the speaker since a separate power supply is not required.

The circuit will respond even to very short peaks making it highly suitable for determining when the amplifier is about to peak (in other words, it

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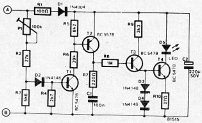


is not just an overload indicator). The peak power level at which the circuit is expected to respond (that is, the peak voltage) is adjustable between 15 and 125 Watts with an 8 ohm speaker (14...45 V). The circuit will light a LED when the amplifier just delivers its peak power enabling the listener to actually see when things begin to go wrong. If the LED only occasionally lights everything is fine. When the LED begins to light continuously then it is time to turn the volume down a little.

The circuit diagram for the indicator is shown in figure 1. Its power supply is derived from capacitor C1 which is charged via R1 and D1 from the speaker output of the amplifier. Half-wave rectification was considered suitable since 'normal' 45 V transistors can be used.

With no signal input all transistors are switched off and therefore current drain from C2 is virtually nil. When the input signal level exceeds a certain value (dependent on the setting of P1), the voltage at the junction of R2 and R3 will reach a point at which T1 will start to conduct.

This switches on T2 causing C1 to charge rapidly. Resistor R7 has been included to prevent the maximum permitted collector current of T2 from being exceeded. Both transistors T3 and T4 will now conduct and LED D5 will light. The current through the LED will be maintained at 20 mA by C2, independent of the speaker signal level. When the input voltage then drops below the preset level, T1 and T2 will switch off. However, the LED will remain lit for a few moments longer while C1 discharges via R7 and R8.

Construction should not present any problems if the printed circuit board shown in figure 2 is used. It would probably be advisable to use the larger type of LED for maximum 'visibility'. Calibration is carried out in the following manner. If the peak power of the amplifier is known, its peak voltage can be calculated with the formula:

$$V_{peak} = 2 \times P_{peak} \times R_{speaker}$$

Connect the indicator circuit to a stabilised power supply (positive to point A), and set the DC supply level to the calculated value. P1 should then be turned back until the LED just begins to light. During this operation care should be taken to ensure that the LED does not remain lit for too long because it may cause the dissipation limit of T4 to be exceeded.

Once the clipping level has been set, the circuit may be connected to one of the speaker outputs of the amplifier or, if desired, to one of the speakers. It may be possible to modify the circuit to operate a relay that rings a bell... or fires a cannon perhaps?

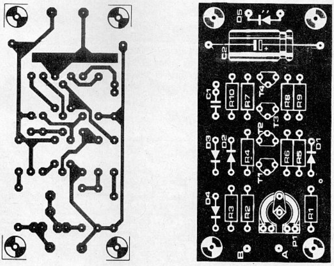
Components required:

Resistors:
R1 = 100 Ω
R2 = 27 k
R3 = 5k6
R4 = 2k7
R5 = 8k2
R6 = 39 k
R7 = 220 Ω
R8 = 1 M
R9 = 3k3
R10 = 27 Ω
P1 = 100 k adjustable potentiometer

Capacitors:
C1 = 100 n
C2 = 220 µ F/50 V

Semiconductors:
D1 = 1N4004
D2, D3, D4 = 1N4148
D5 = LED
T1, T3, T4 = BC 547B
T2 = BC 557B

2



6502 Tracer

A program that has been written into an assembler will rarely run error free on the first run. It often exhibits blurbs and other ramblings: in bad cases, there is a complete hang up and it is then necessary to start the computer afresh with a RESET.

To find such faults in a relatively easy manner, the tracer described here will be found very useful.

The circuit layout of the tracer is shown in figure 1. Gate N_1 is an address decoder, whose output in the address range $F000...$FFFF is logic 0. NAND gate N_2 is fed with the SYNC signal from the computer and the 0 signal; it is disabled by either the address decoder, N_1, or bistable FF_2. The address decoder disables N_2 when the EPROM is addressed from the CPU. This prevents the SYNC line of the 6502 processor generating an MI (maskable interrupt). If the processor passes through a machine program somewhere in the RAM, N₂ generates an interrupt as soon as the processor reads an opcode, which makes the SYNC line logic 1. This non-maskable interrupt directs the processor to an interrupt program in the monitor program. All CPU registers are safeguarded by this interrupt program and subsequently displayed on the monitor screen. At the same time, the processor disassembles the next command.

The programmer can, therefore, see beforehand under what conditions the processor starts with the execution of the next opcode. Since the status register and all its flags are also displayed on the screen, the programmer can easily ascertain whether a flag in the status register has been set incorrectly.

Bistable FF₁ serves as a debounce stage; FF₂ toggles on receipt of a leading edge from FF₁: that is, every time S₁ is pressed. When the tracer is switched on, D₁ lights. Resistor *R*₄ and capacitor *C*₁ form a power-on reset network that automatically switches the tracer off when the computer is switched on.

The printed circuit board for the tracer is shown in figure 2. If you want to build the tracer into the computer case, the PCB can be cut along the dashed line, so that the section containing S₁ and S₂ may be fitted in the most convenient position. Switch S₁ must be connected to the tracer via a suitable cable, but S₂ may be connected to the manual RESET of the system.

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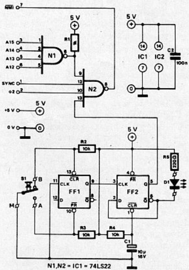

N1,N2 = IC1 = 74LS22
FF1,FF2 = IC2 = 74LS74

Parts list

Resistors:
R₁ = 1 k
R₂ . . . R₄ = 10 k
R₅ = 220 Ω

Capacitors:
C₁ = 10 μ/16 V
C₂ = 100 n

Semiconductors:
D₁ = LED (red)
IC₁ = 74LS22
IC₂ = 74LS74

Miscellaneous:
S₁ = miniature spring-loaded press-to-make switch
S₂ = miniature spring-loaded press-to-make switch (see text)
PCB 85466

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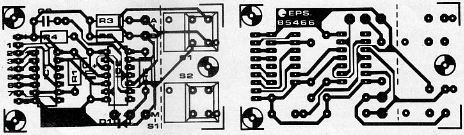

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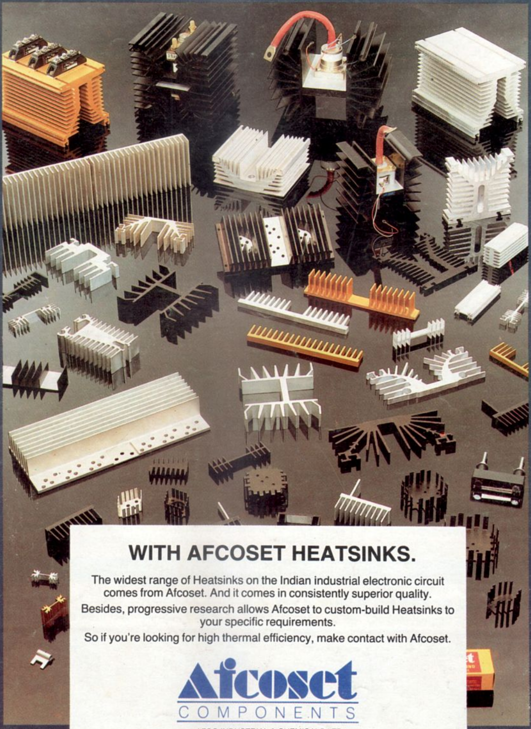

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